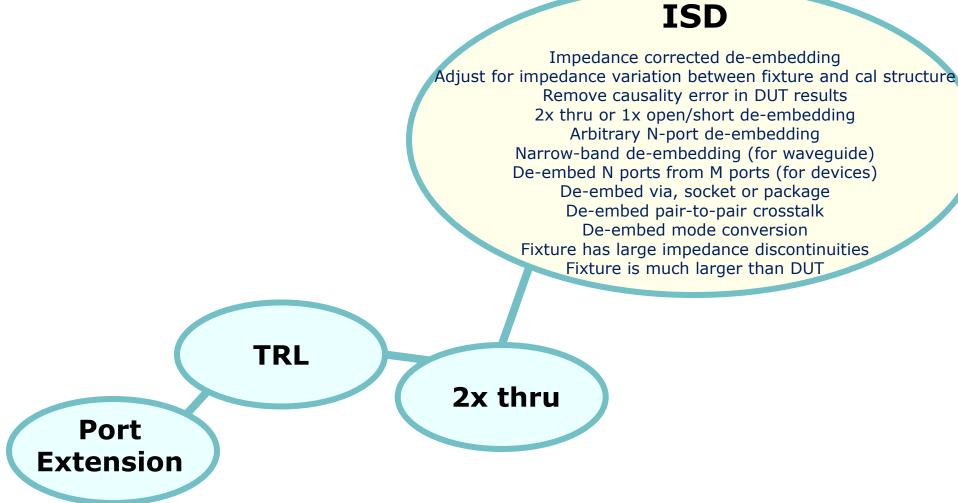
## In-Situ De-embedding (ISD)

Ching-Chao Huang huang@ataitec.com

April 28, 2025



## Fixture removal has come a long way





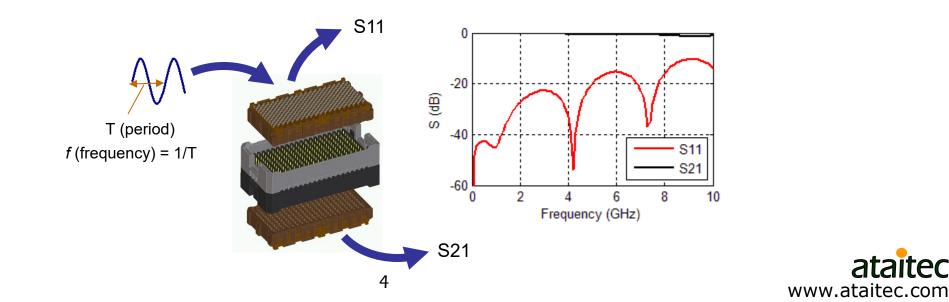
## Outline

- What is causality
- What is In-Situ De-embedding (ISD)
- Comparison of ISD results with simulation and other tools
- How non-causal de-embedding affects connector compliance testing
- How to extract accurate PCB trace attenuation that is free of spikes and glitches
- How to extract a PCB's material property (DK, DF, roughness) by matching all IL, RL, NEXT, FEXT and TDR/TDT of de-embedded PCB traces
- New "Smoothing" feature for better accuracy to higher frequencies
- Automated PCIe 5.0 and ccICN compliance testing



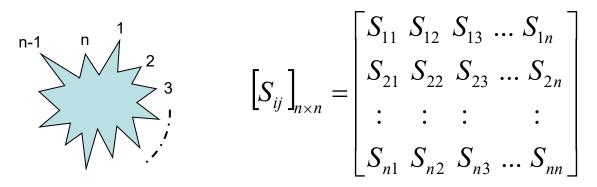
## **VNA and S parameter**

- Vector network analyzer (VNA) is an equipment that launches a sinusoidal waveform into a structure, varies the period (or frequency) of waveform, and lets us observe the transmitted and reflected wave as "frequency-domain response".
- Such frequency-domain response, when normalized to the incident wave, is called scattering parameter (or, S parameter).



## What is S parameter

For an n-port (or I/O) device, S parameter is an n x n matrix:



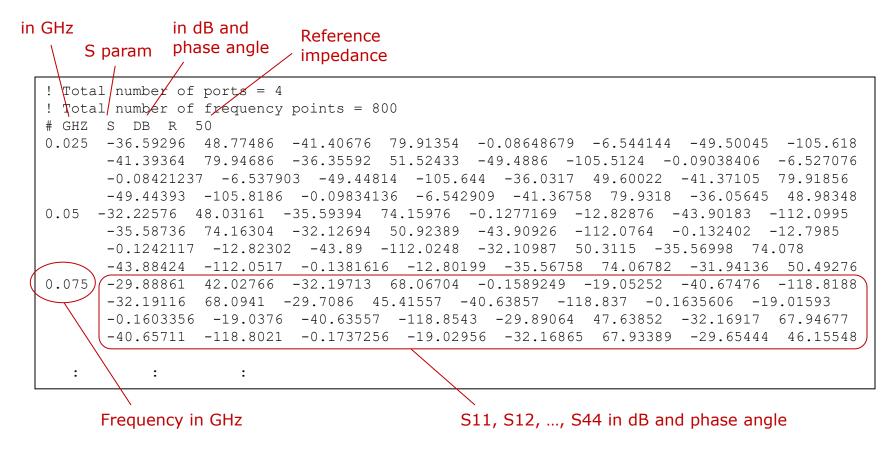
- Sij is called the S parameter from Port j to Port i.
- Sij has a unique property that its magnitude is less than or equal to 1 (or, 0 dB) for a passive device.

$$\begin{vmatrix} S_{ij} \end{vmatrix} \leq 1$$
  
$$S_{ij} (dB) = 20 \times \log_{10} |S_{ij}| \leq 0 \ dB$$



## What is a Touchstone (.sNp) file

S parameter at each frequency is expressed in Touchstone file format.





## What is causality

#### cau·sal·i·ty /kôˈzalədē/

noun

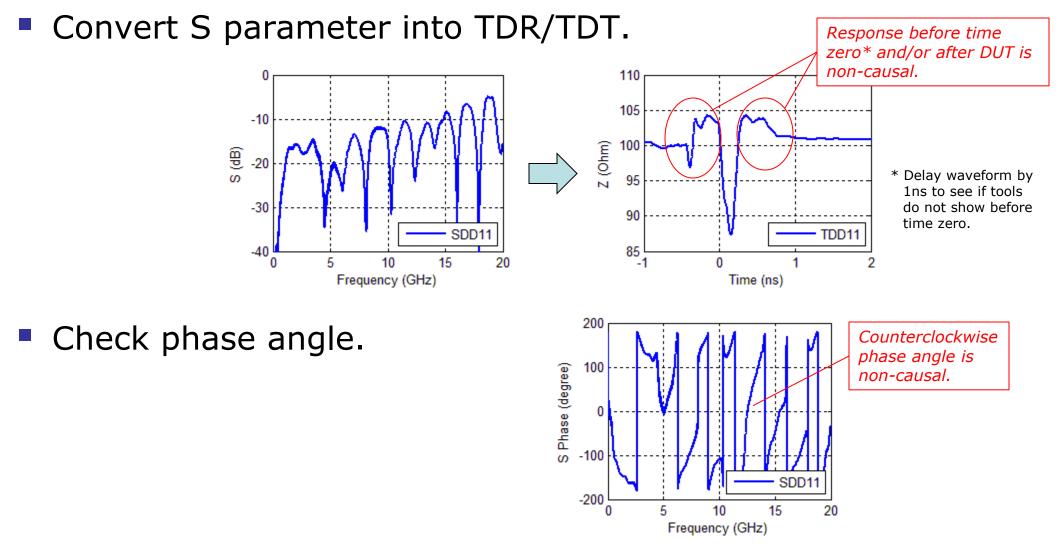
- 1. the relationship between cause and effect.
- 2. the principle that everything has a cause.

In other words:

Can not get something from nothing.



## How to identify non-causal S parameter



## Why does S parameter violate causality

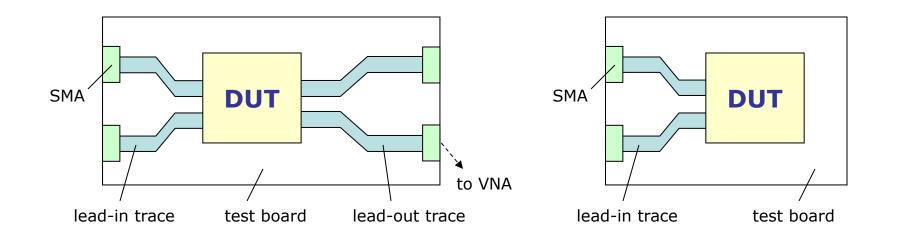
- Measurement error (de-embedding), simulation error (material property) and finite bandwidth of S parameter all contribute to noncausality.
- Kramers-Kronig relations require that the real and imaginary parts of an analytic function be related to each other through Hilbert transform:

$$\Psi(\omega) = \Psi_{R}(\omega) + j\Psi_{I}(\omega)$$
$$\Psi_{R}(\omega) = \frac{1}{\pi} P \int_{-\infty}^{\infty} \frac{\Psi_{I}(\omega')}{\omega' - \omega} d\omega'$$
$$\Psi_{I}(\omega) = -\frac{1}{\pi} P \int_{-\infty}^{\infty} \frac{\Psi_{R}(\omega')}{\omega' - \omega} d\omega'$$



## What is de-embedding

To remove the effect of fixture (SMA connector + lead-in/out) and extract the S parameter of DUT (device under test).

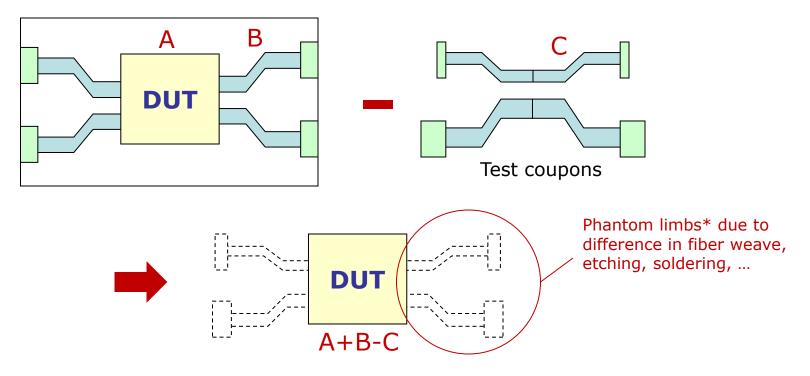


- The lead-ins and lead-outs don't need to look the same.
- There may even be no lead-outs (e.g., package).



## Why do most de-embedding tools give causality error

 Most tools use test coupons directly for de-embedding, so difference between actual fixture and test coupons gets piled up into DUT results.

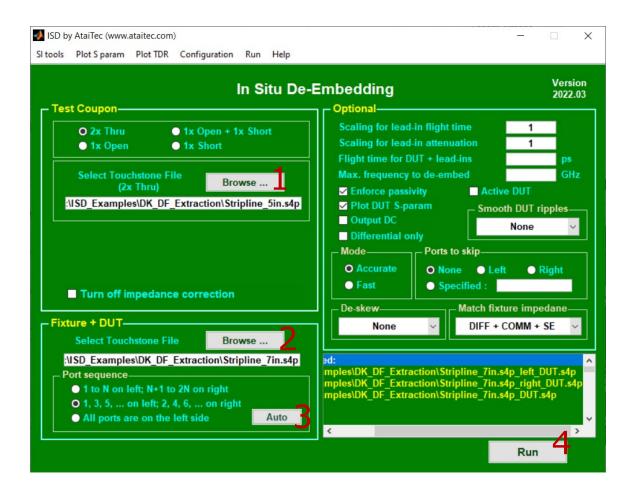


\* <u>http://www.edn.com/electronics-blogs/test-voices/4438677/Software-tool-fixes-some-causality-violations</u> by Eric Bogatin



#### What is In-Situ De-embedding (ISD) Introduced to address impedance variation

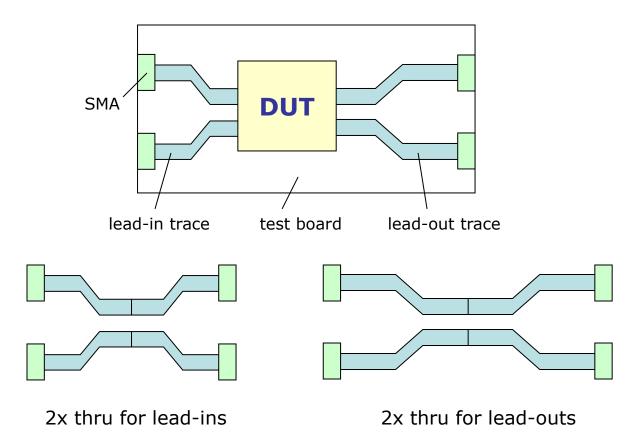
- ISD uses test coupon ("2x thru" or "1x open / 1x short") as reference and deembeds fixture's actual impedance through numerical optimization.
- Other tools use test coupon directly for de-embedding and give causality error when test coupon and actual fixture have different impedance.
- ISD addresses impedance variation between test coupon and actual fixture through software, instead of hardware, improving de-embedding accuracy and reducing hardware cost.





## What is "2x thru"

"2x thru" is 2x lead-ins or lead-outs.

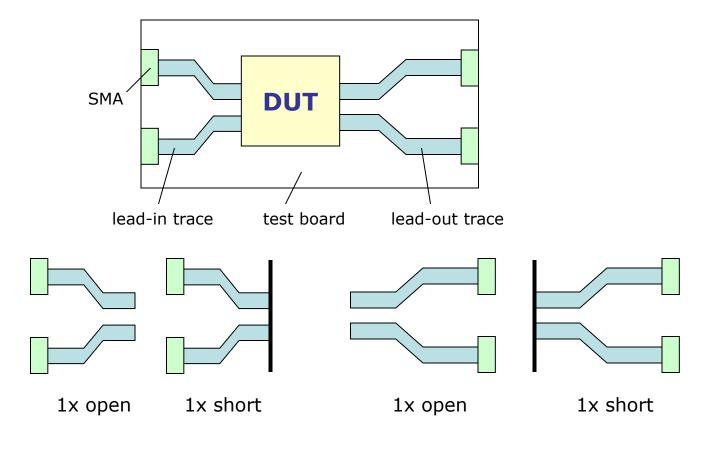


2 sets of "2x thru" are required for asymmetric fixture.



## What is "1x open / 1x short"

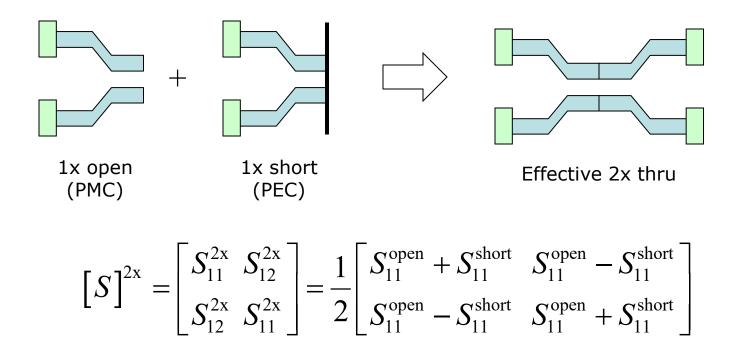
"1x open / 1x short" is useful when "2x thru" is not possible (e.g., connector vias, socket, package, ...).





## What is "1x open + 1x short"

"1x open + 1x short" can be equated to effective\* 2x thru.



\* C.C. Huang, "Fixture de-embedding using calibration structures with open and short terminations," US patent no. 10761175B2, Sep. 1, 2020.



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## **ISD advantages**

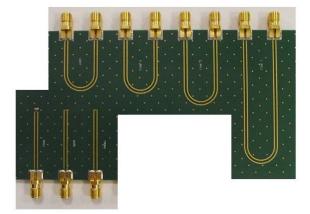
	ISD	Others
Accuracy	Accurate and causal DUT results. Easier to correlate with simulation, improving design and time to market.	Artificial ripples in S-param; non-physical TDR/TDT before and after DUT. Difficult to correlate with simulation, resulting in long design cycle.
Cost saving	Saves hardware cost because inexpensive test fixtures with large impedance variation can be used.	Requires expensive test fixtures to tighten impedance variation.
	Precise qualification in meeting compliance spec. Avoid components from being thrown away by mistake.	Good components may fail compliance spec because of de-embedding error and get thrown away by mistake.
Technology	Uses impedance corrected 2x thru or 1x open/short to de-embed actual fixture impedance	Uses 2x thru or 1x open/short to directly de-embed fixture, resulting in causality error.
Capabilities	Able to de-embed arbitrary number of ports.	No
	Able to de-embed n ports from m-port structures (n<=m and n, m are arbitrary). Essential for RF and MEMS devices.	No
	Able to de-embed mode conversion	No
	Able to use single line to de-embed crosstalk	No
	Able to de-embed longer or shorter than existing test coupons	No
	Automatic de-skew	No
	Creates effective 2x thru from 1x open + 1x short	No
	Extracts small DUT from a large board	Error is extremely large if DUT is much smaller than test fixture.
	De-embeds asymmetric structures	Claims to be able to de-embed asymmetric structures but assumes IL to be identical on both left and right sides of test fixture.

\* See <u>https://ataitec.com/docs/ISD\_advantages.pdf</u> for a complete list.



## Why ISD is more accurate and saves \$\$\$

#### TRL calibration board



- More board space Multiple test coupons are required.
- Test coupons are used directly for de-embedding.
- All difference between actual fixture and test coupons gets piled up into DUT results.
- Expensive SMAs, board materials (Roger) and tightetching-tolerance are required.
  - Impossible to guarantee all SMAs and traces are identical (consider weaves, etching, ...)
- Time-consuming manual calibration is required.
  - Reference plane is in front of DUT.

#### ISD test coupon

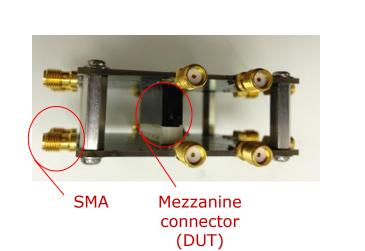


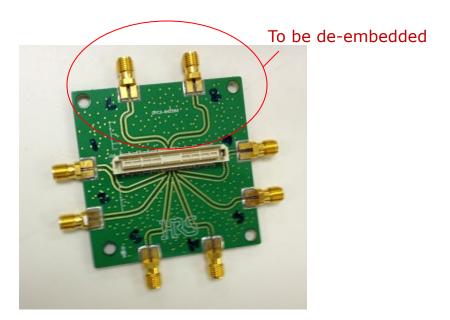
- Only one 2x thru test coupon is needed.
- Test coupon is used only for reference, not for direct de-embedding.
- Actual fixture impedance is de-embedded.
- Inexpensive SMAs, board materials (FR4) and looseetching-tolerance can be used.
- ECal can be used for fast SOLT calibration.
  - Reference plane is in front of SMA.
  - De-embedding requires only two input files: 2x thru and DUT board (SMA-to-SMA) Touchstone files.
  - Both de-embedding and DUT files are provided as outputs.

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#### **Example 1: Mezzanine connector** *ISD vs. TRL*

In this example, we will use ISD and TRL to extract a mezzanine connector and compare their results.



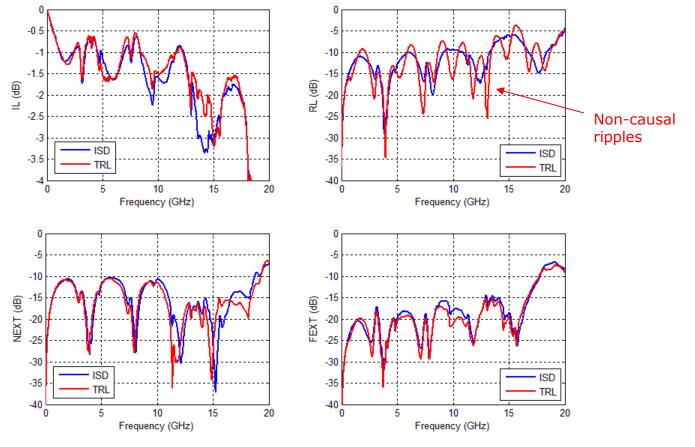


\*Courtesy of Hirose Electric



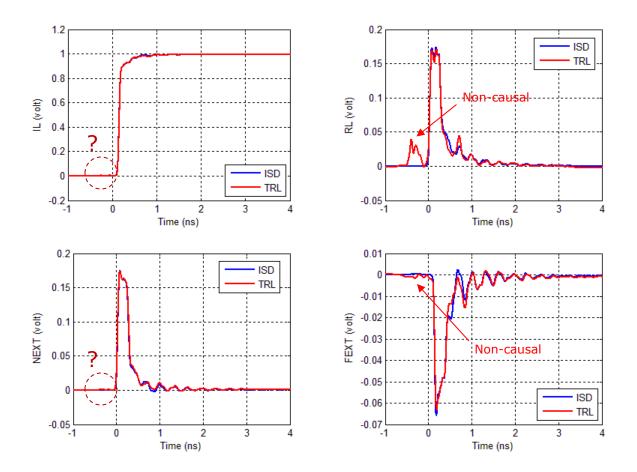
#### **DUT results after ISD and TRL** *Which one is more accurate?*

TRL gives too many ripples in return loss (RL) for such a small DUT.





#### **Converting S parameter into TDR/TDT shows noncausality in TRL results**

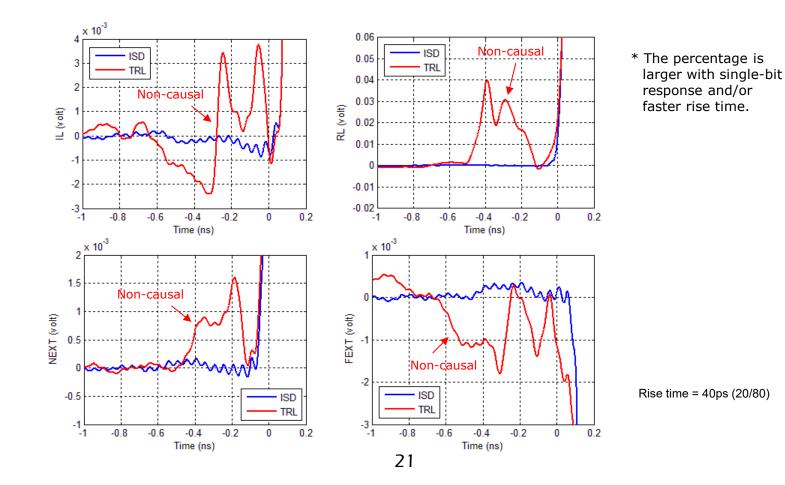


Rise time = 40ps (20/80)



# Zoom-in shows non-causal TRL results in all IL, RL, NEXT and FEXT

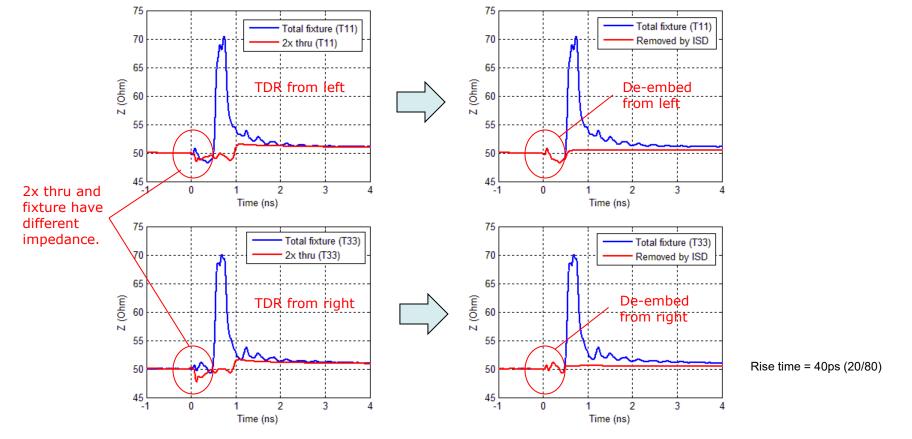
TRL causes time-domain errors of 0.38% (IL), 25.81% (RL), 1.05% (NEXT) and 2.86% (FEXT) in this case\*.





## How did ISD do it?

Through numerical optimization, ISD de-embeds fixture's impedance exactly, independent of 2x thru's impedance.

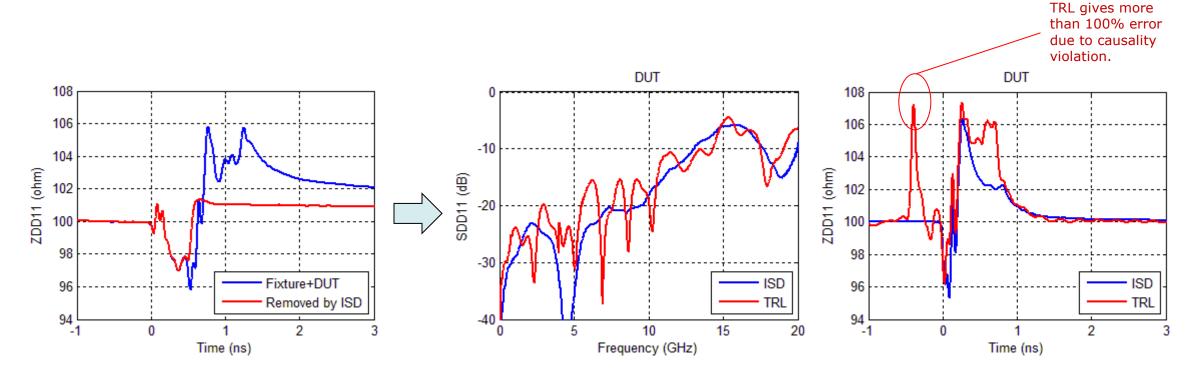




### TRL can give huge error in SDD11 even with less than **5% impedance variation\***

\* See previous slide.

ISD is able to de-embed fixture's differential impedance with only a single-trace 2x thru.

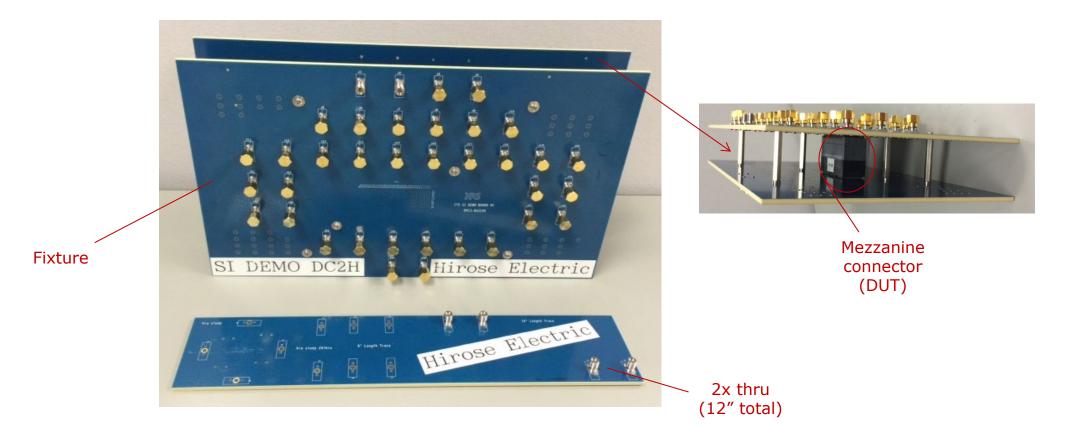


Rise time = 40ps(20/80)



#### **Example 2: Mezzanine connector** *Extracting DUT from a large board*

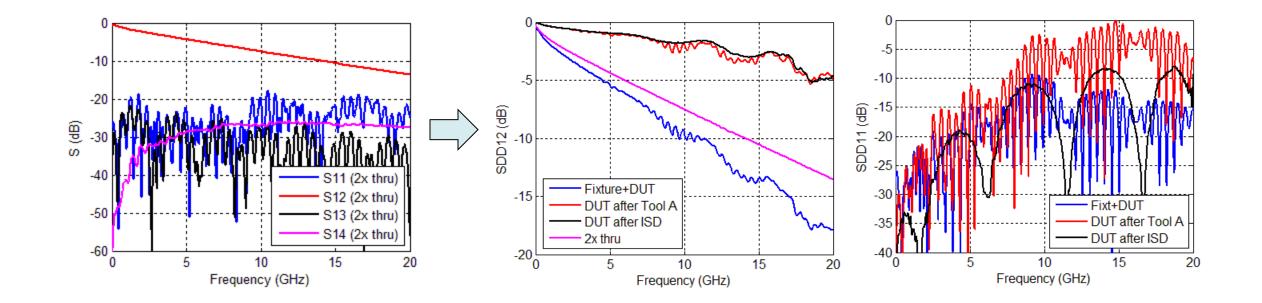
TRL is impractical for de-embedding large and coupled lead-ins/outs.





### **ISD** can use a .s4p file of 2x thru for de-embedding

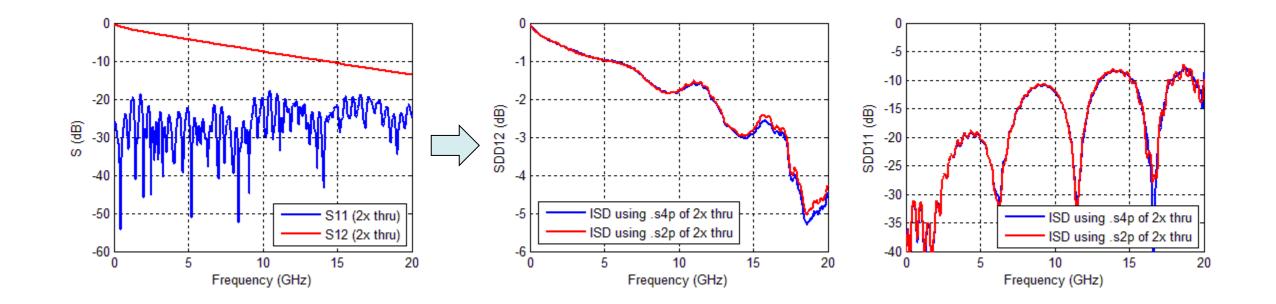
- TRL would have required many long and coupled traces.
- "Tool A" gave incorrect results.





# ISD can even use a .s2p file of 2x thru to de-embed crosstalk...

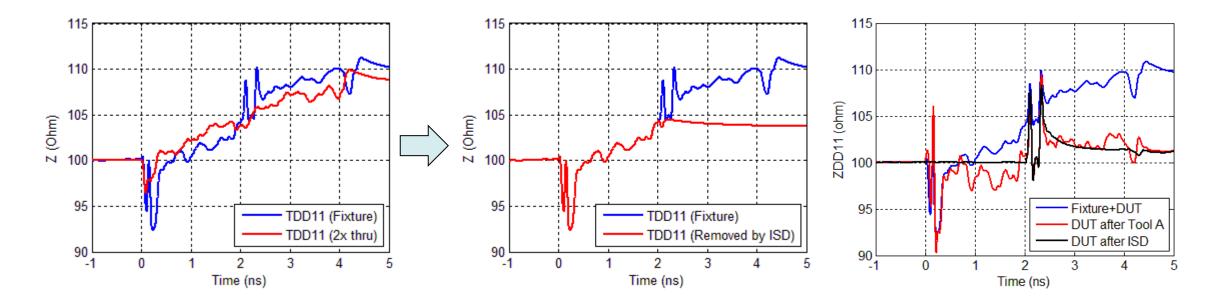
And the results are similar!





# **ISD** allows a large demo board to double as a characterization board

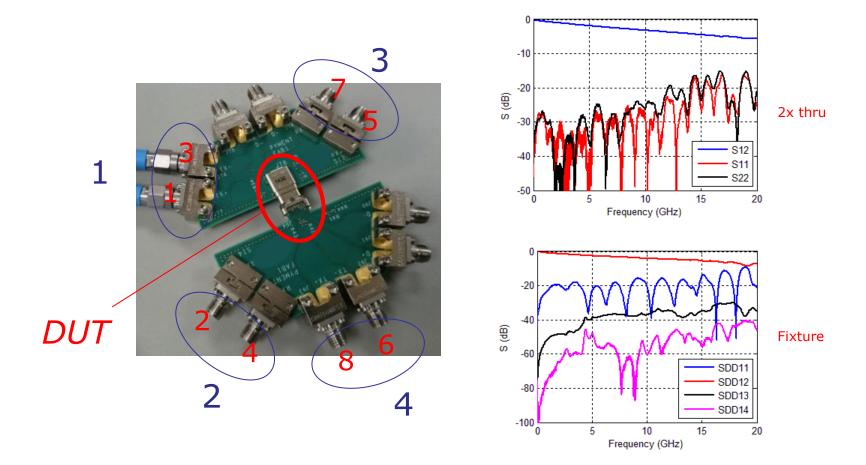
- ISD de-embeds fixture's impedance regardless of 2x thru's impedance.
- "Tool A" gave causality error before and after DUT.





#### **Example 3: USB type C mated connector** *ISD vs. Tool A*

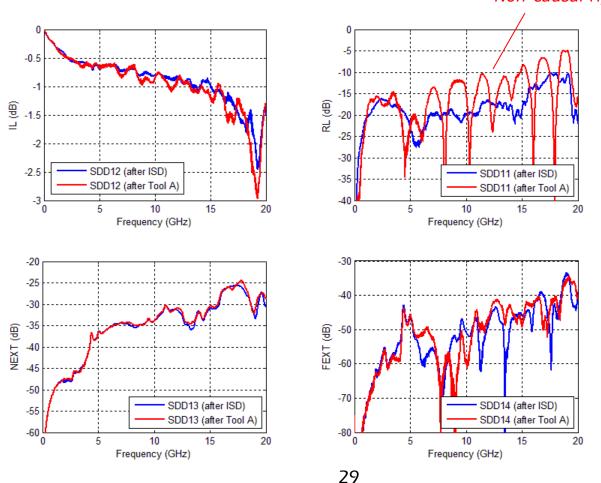
Good de-embedding is crucial for meeting compliance spec.





#### **DUT results after ISD and Tool A** *Which one is more accurate?*

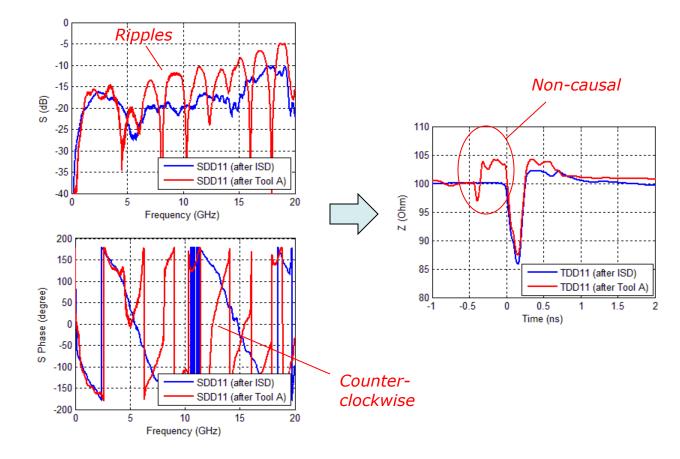
"Tool A" gives too many ripples in return loss (RL) for such a small DUT.
Non-causal ripples





#### **Converting S parameter into TDR/TDT shows noncausality in Tool A results**

 Counter-clockwise phase angle is another indication of noncausality.



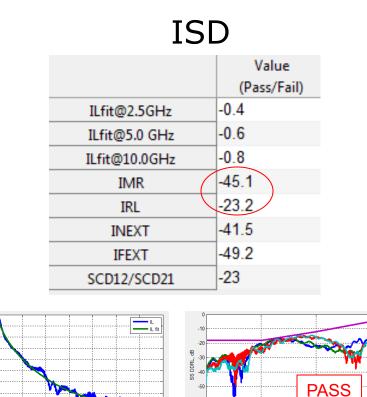


### **De-embedding affects pass or fail of compliance spec.**

ISD improves IMR and IRL (from compliance tool).

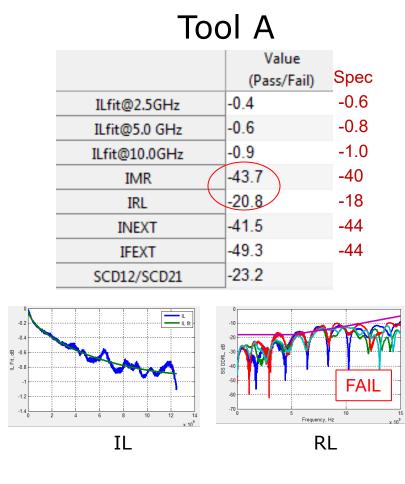
Frequency, Hz

RL



뜅 -0.4

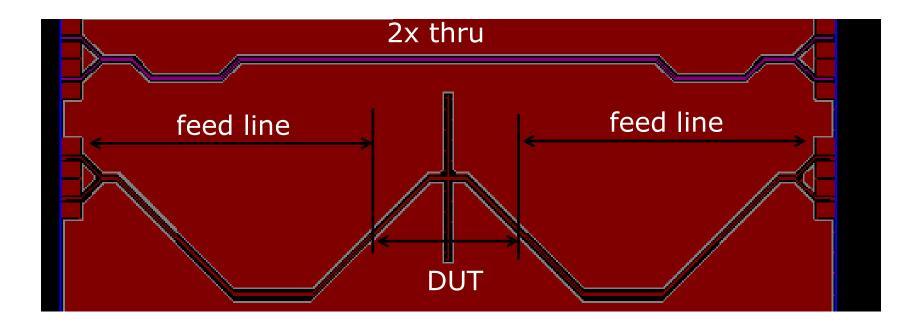
IL





#### **Example 4: Resonator** *ISD vs. Tool A vs. simulation*

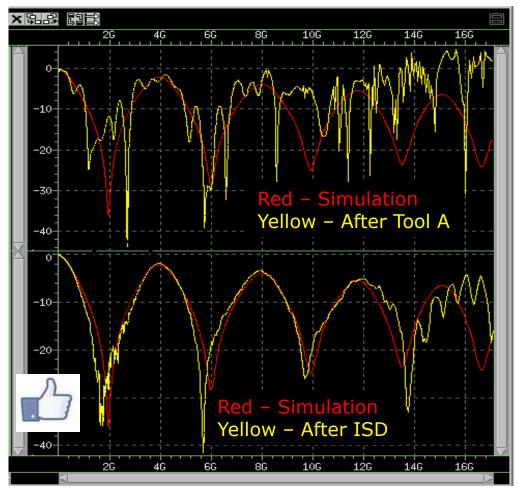
Good de-embedding is crucial for design verification (i.e., correlation) and improvement.

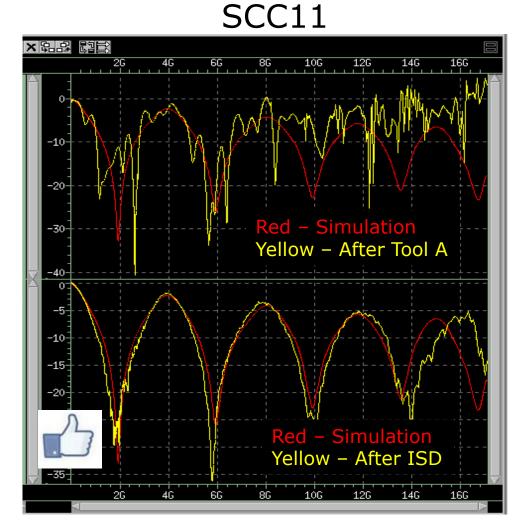




#### **ISD correlates with simulation** *Good correlation is crucial for design improvement*

SDD11

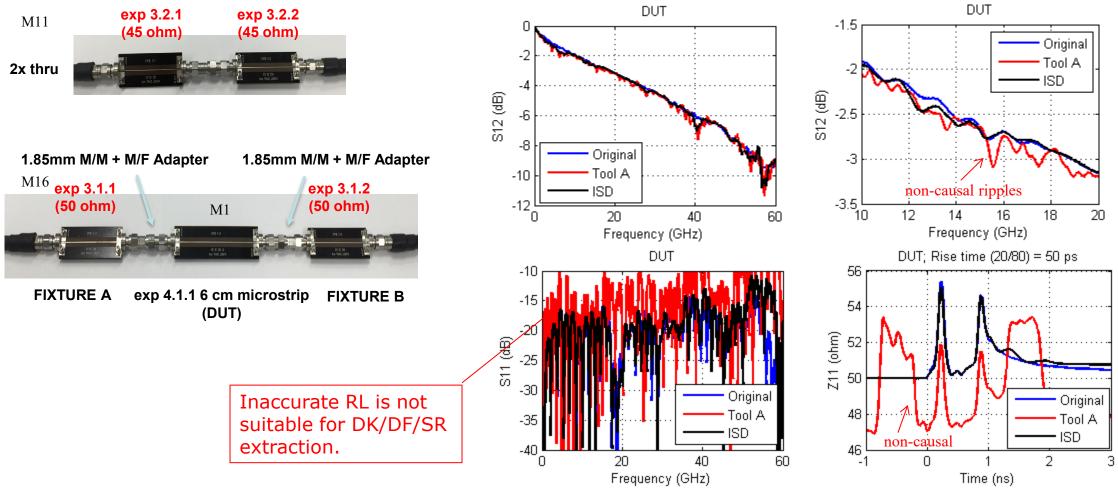






#### **Example 5: IEEE P370 plug and play kit** *Using 45 ohm 2x thru to de-embed 50 ohm fixture*\*

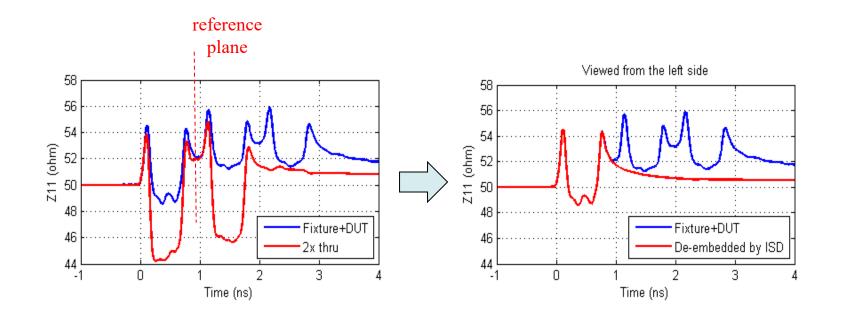
\* To mimic possible PCB impedance variation





## **2x thru vs. fixture impedance**

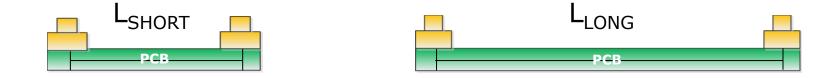
ISD de-embeds fixture's impedance, not 2x thru's impedance.

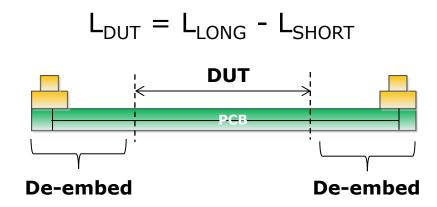




#### **Example 6: PCB trace attenuation** *ISD vs. eigenvalue (Delta-L)*

De-embed short trace ( + launch) from long trace ( + launch) to get trace-only attenuation.

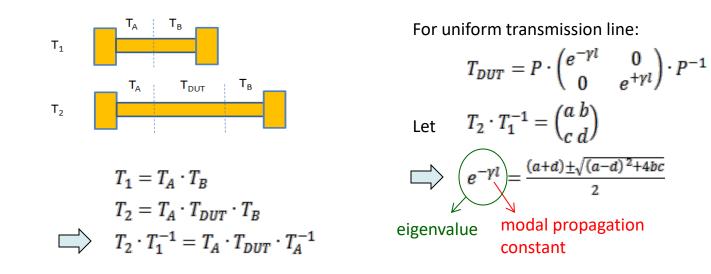






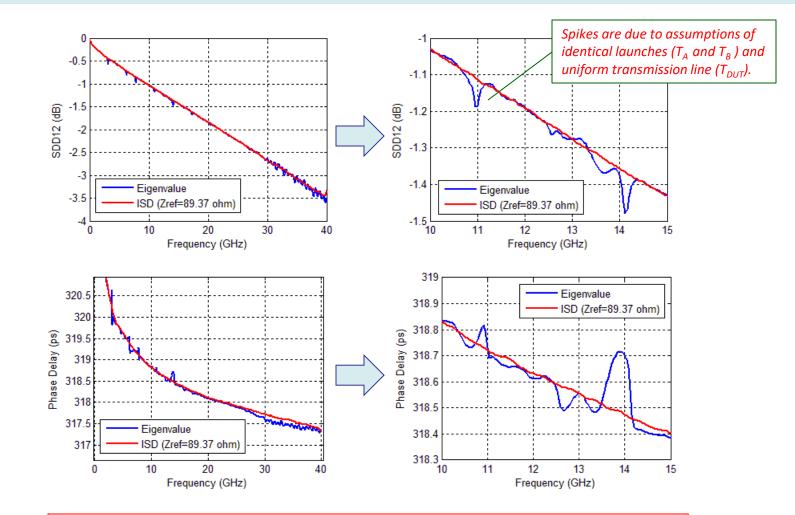
### **Eigenvalue solution: not de-embedding** *For calculating trace attenuation only*

- Convert S to T for short and long trace structures
- Assume the left (and right) sides of short and long trace structures are identical
- Assume DUT is uniform transmission line
- Trace-only attenuation is written in one equation.





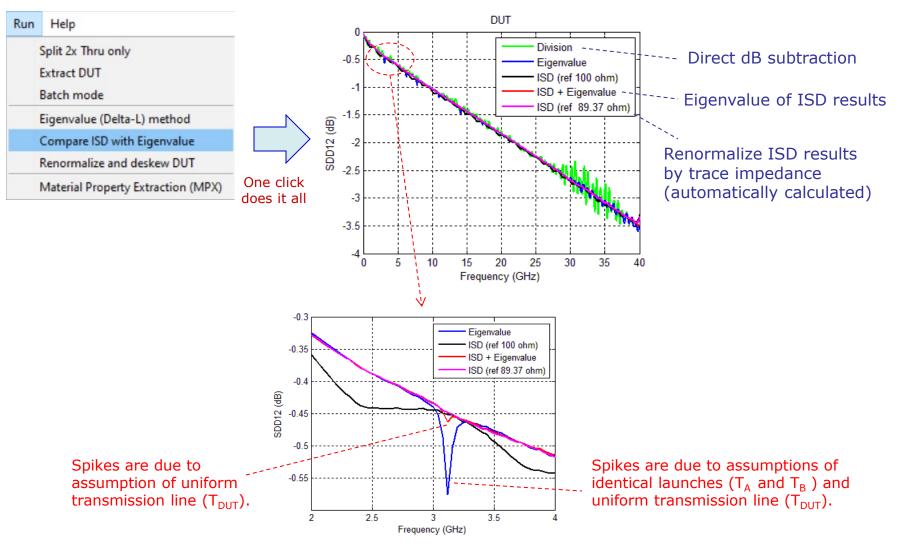
#### **Case 1: 2" (=7"-5") trace attenuation** *Eigenvalue solution is prone to spikes*



ISD's spikes-free results help DK and DF extraction later.



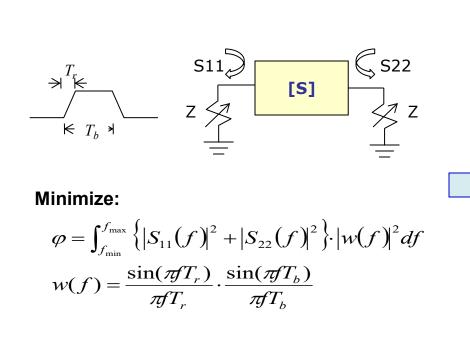
## **One click compares ISD with eigenvalue and more...**



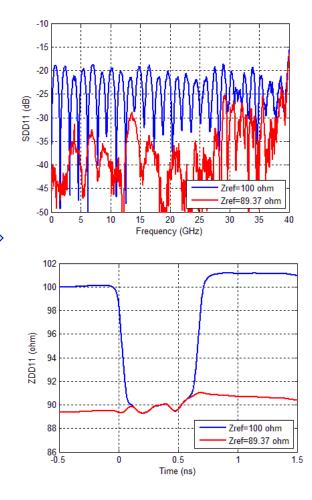


### How to define trace impedance PCB trace is non-uniform transmission line

Define impedance by minimal RL\*



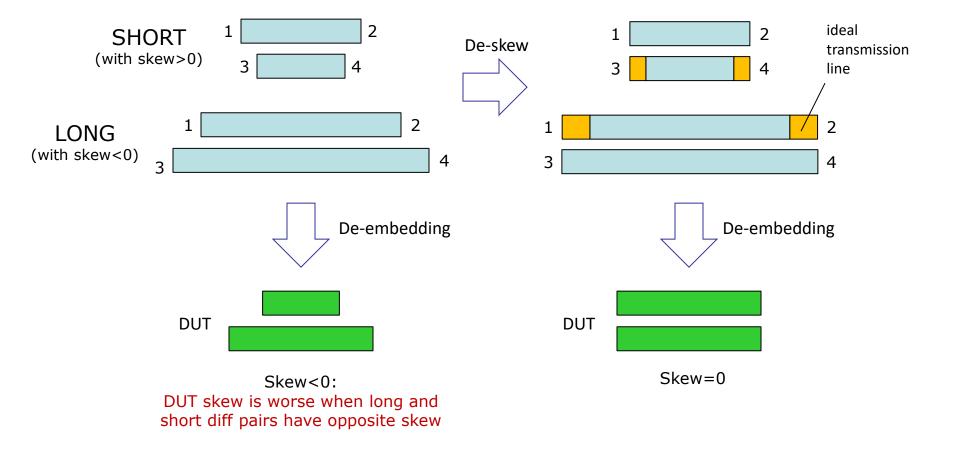
\* J. Balachandran, K. Cai, Y. Sun, R. Shi, G. Zhang, C.C. Huang and B. Sen, "Aristotle: A fully automated SI platform for PCB material characterization," DesignCon 2017, 01/31-02/02/2017, Santa Clara, CA.





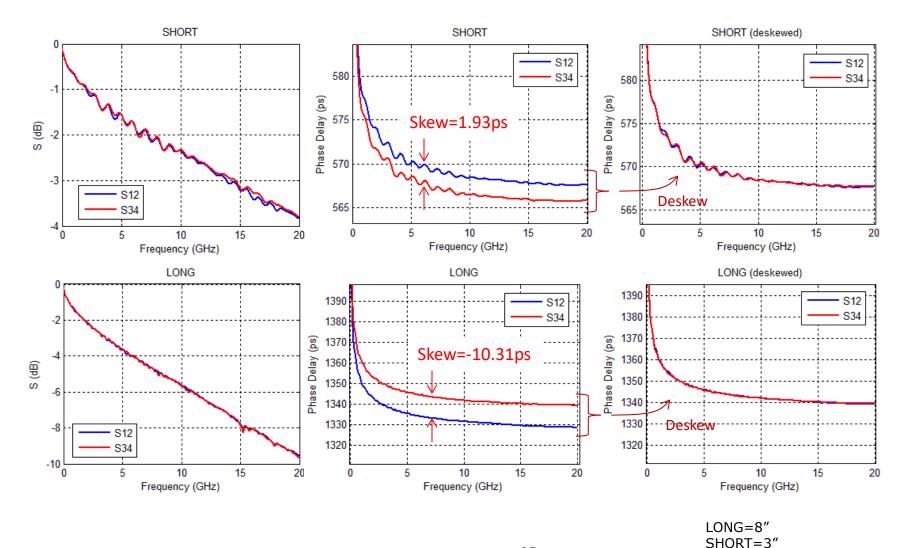
# **Skewless de-embedding**

Pad ideal transmission line to de-skew.





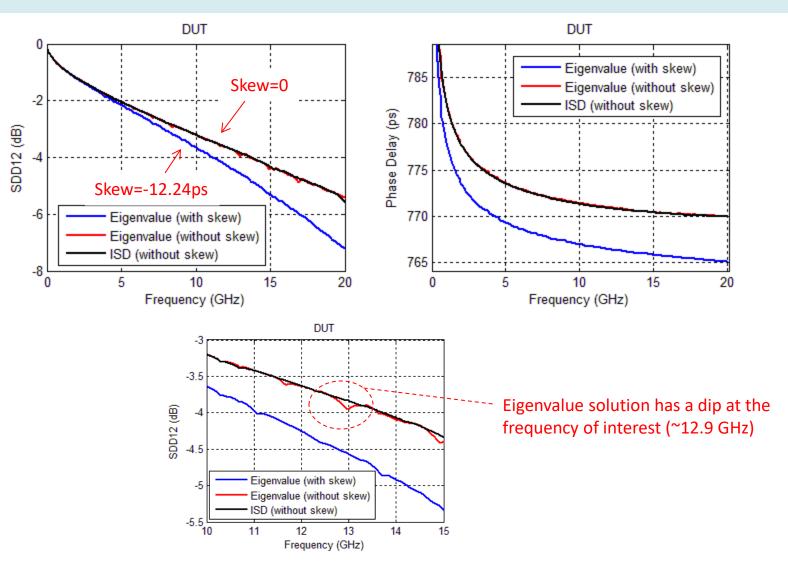
## ISD optionally automates de-skewing of raw data





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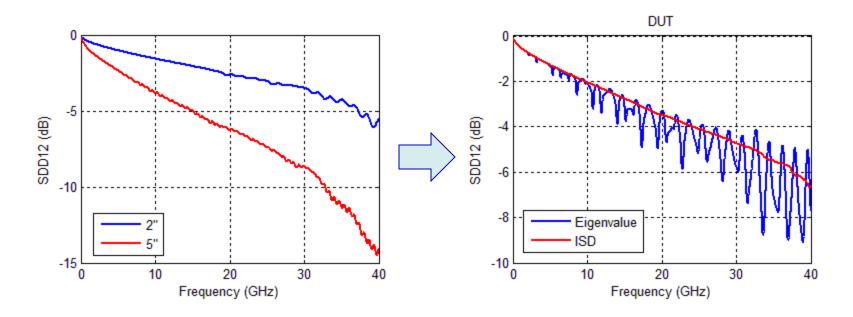
## **Case 2: Extracted trace attenuation can be very different with or without skew**





# **Case 3: Eigenvalue (Delta-L) solution becomes unstable in this case, but why?**

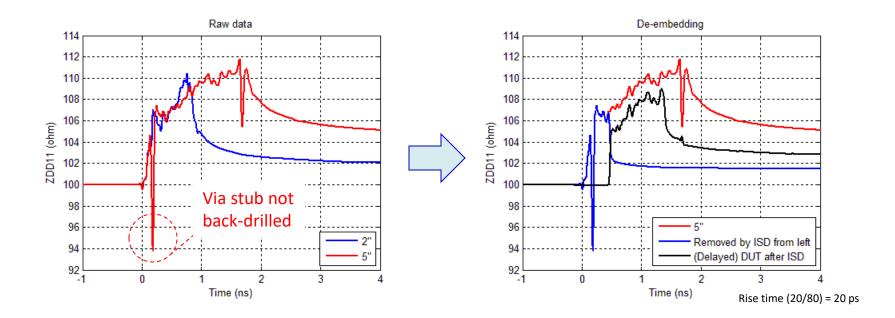






### **TDR of raw data reveals why...** 2" structure was back-drilled but 5" was not

- Eigenvalue solution assumes 2" and 5" structures have identical launches.
- ISD de-embeds 5" structure's launch correctly.

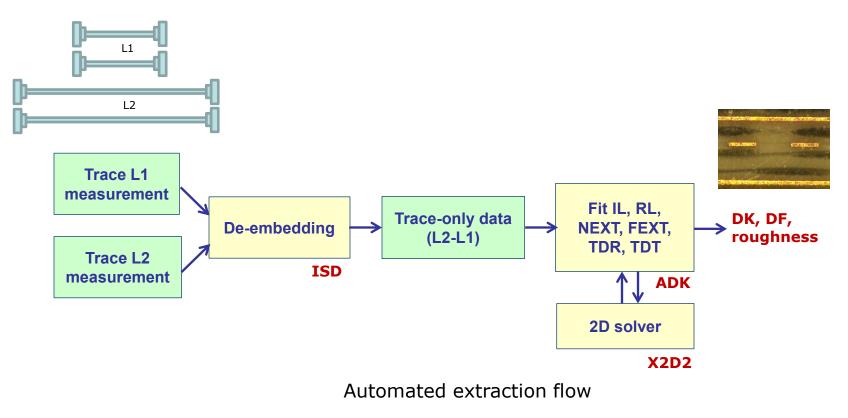


ISD saves \$\$\$ and time for not spinning another board.



## **Example 7: Material property extraction** *DK, DF and roughness*

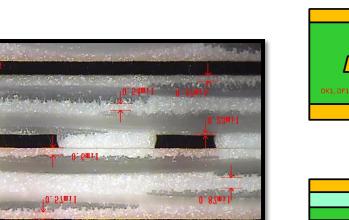
Self consistent approach to extract DK, DF and roughness by matching all IL, RL, NEXT, FEXT and TDR/TDT of de-embedded trace-only data.



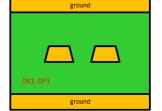


## **Models for cross section**

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Model 1

ground DK2, DF2 R1 R3 R4 DK1, DF1 R5 ground

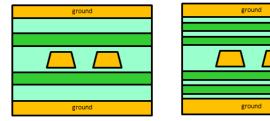
Model 2

Optimized variables: DK1, DF1, DK2, DF2

R1, R2, R3, R4, R5 (roughness) Metal width and spacing

	grou	nd	
DK1, DF1			
DK2 DF2			
DK1, DF1			
ground			

Model 3



Model 4

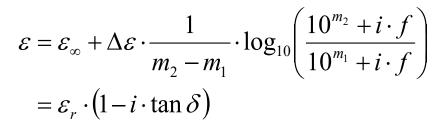
Model 5

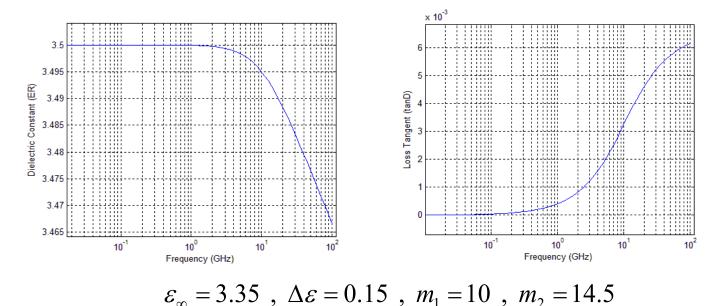


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# **Causal dielectric model**

- Wideband Debye (or Djordjevic-Sarkar) model
  - Need only four variables:  $\varepsilon_{\infty}$  ,  $\Delta \varepsilon$  ,  $m_1$  ,  $m_2$



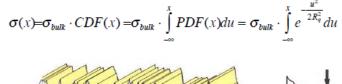




# **Surface roughness model**

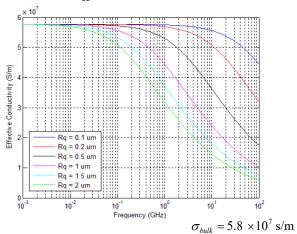
• Effective conductivity (by G. Gold & K. Helmreich at DesignCon 2014) needs only two variables:  $\sigma_{bulk}$ ,  $R_q$ 

Parameter	Description	Standard	
$R_q$	root mean square	DIN EN ISO 4287	
Ra	arithmetic average	DIN EN ISO 4287, ANSI B 46.1	
Rk	core roughness depth	DIN EN ISO 13565	
Rz	average surface roughness	DIN EN ISO 4287	





• Numerically solving  $\nabla^2 \overline{B} - j\omega\mu\sigma\overline{B} + \frac{\nabla\sigma}{\sigma} \times (\nabla \times \overline{B}) = 0$  and equating power to that of smooth surface gives  $\sigma_{eff}$ 



- ✤ Simple
- Work well with field solver
- Give effect of roughness on all IL, RL, NEXT and FEXT



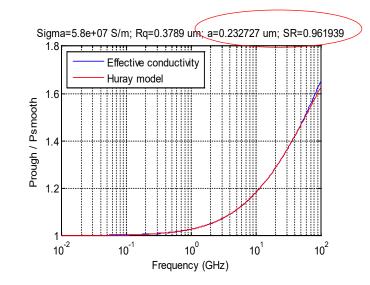
Table 1: Statistical parameters to describe surface roughness

# **Convert effective conductivity to Huray model**

Huray model

$$\frac{P_{rough}}{P_{smooth}} \approx 1 + \frac{3}{2} \cdot SR \cdot \left( \frac{1}{1 + \frac{\delta(f)}{a} + \frac{1}{2} \left( \frac{\delta(f)}{a} \right)^2} \right)$$
$$\delta(f) = \sqrt{\frac{1}{\pi f \mu \sigma}} \quad ; \quad a = \text{radius} \quad ; \quad SR = \text{surface ratio}$$

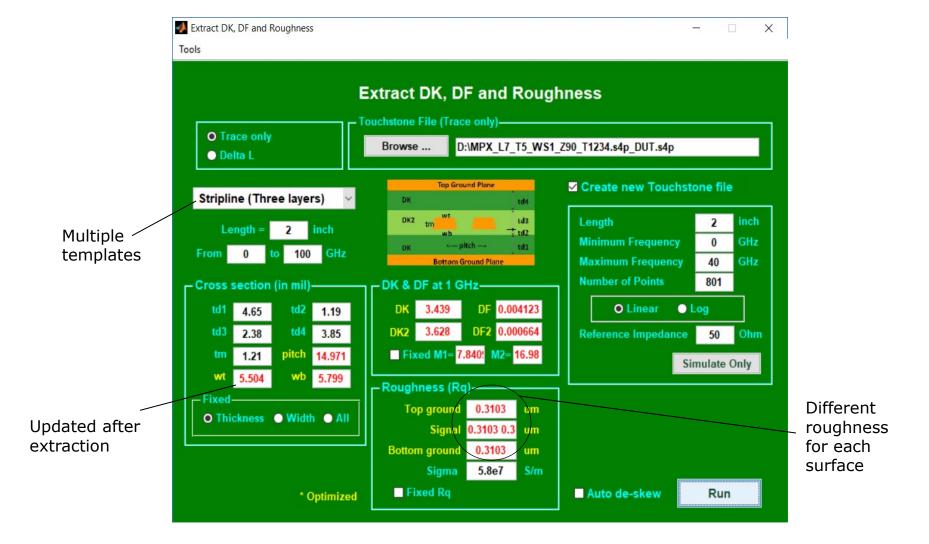
• Curvefit\* Prough / Psmooth to convert  $\sigma_{bulk}$ ,  $R_q$  to a, SR



\*Automated in ADK



# **DK/DF/SR extraction (from ADK)**

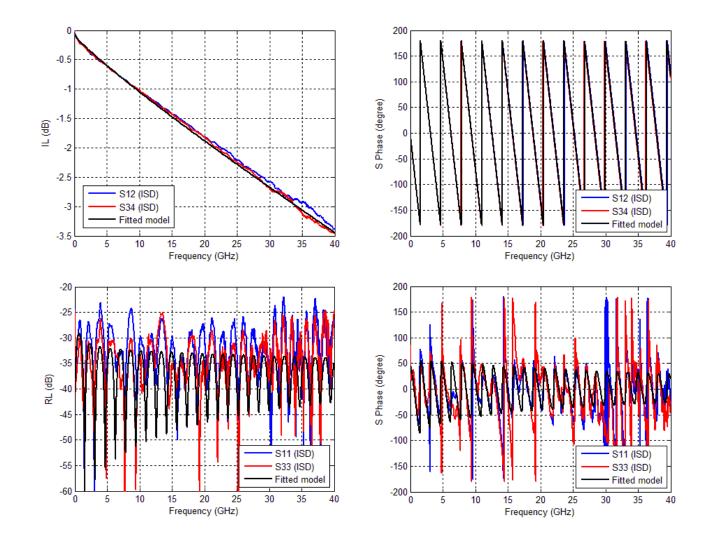


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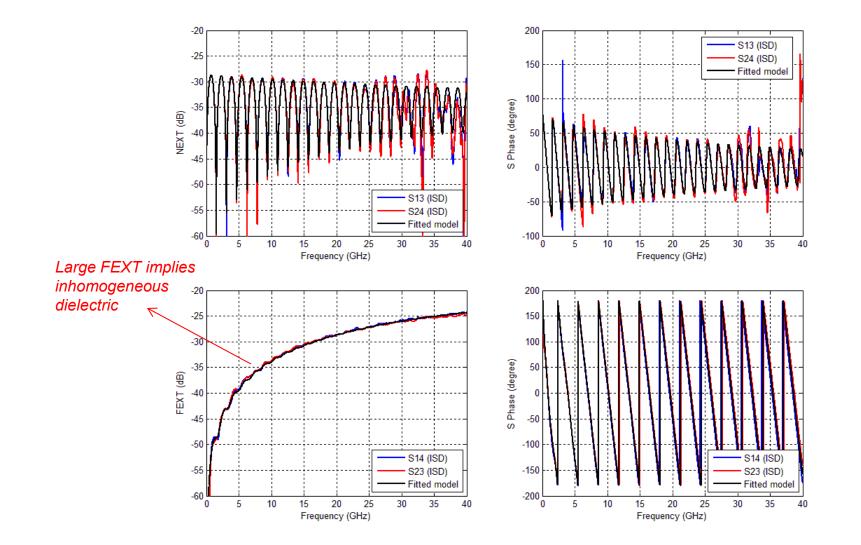
# Matching IL and RL





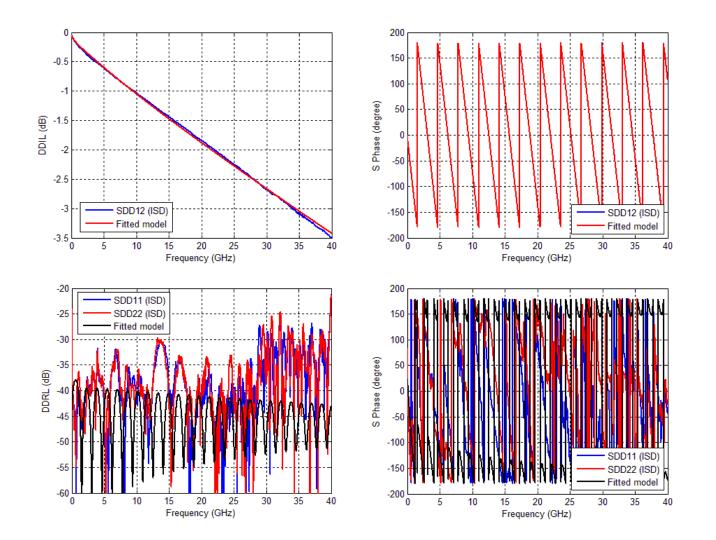
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# **Matching NEXT and FEXT**



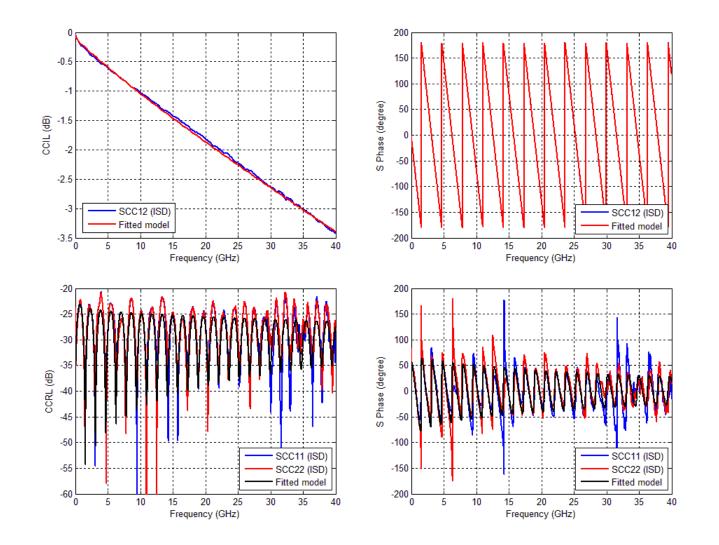


# **Matching DDIL and DDRL**



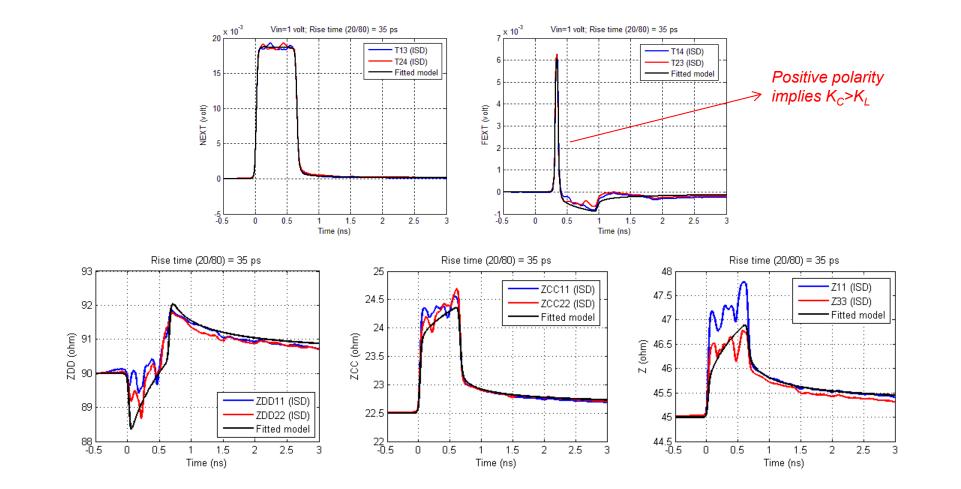


# **Matching CCIL and CCRL**





# **Matching TDT and TDR**



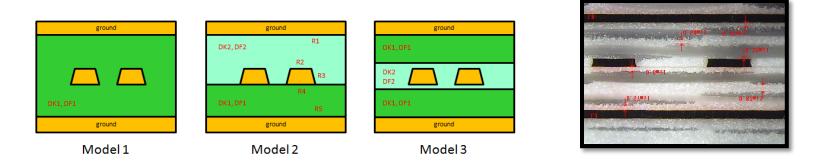


# **Comparison of Models 1 to 5**

DK2

DK1

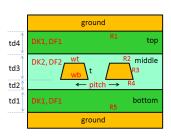
Model 1 cannot match FEXT. Models 2 to 5 can match all IL, RL, NEXT, FEXT and TDR/TDT very well.



ground	ground	Model	DK1	DK2	DK2>DK1 because of positive-polarity
		1	3.510	-	✓ FEXT
		2	2.444	4.294	TEXT
		3	3.413	3.623	$\rightarrow$
		4	3.863	3.360	
ground	ground	5	3.115	3.975	
Model 4	Model 5			At 10 GHz	

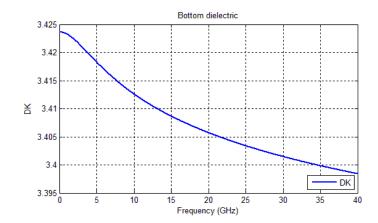


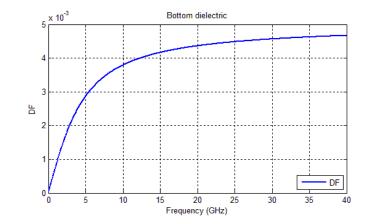
### **Extracted DK1 and DF1** *Model 3*



 $\varepsilon_{\infty} = 3.27929$   $\Delta \varepsilon = 0.144348$  m1 = 9.58619m2 = 15.4109

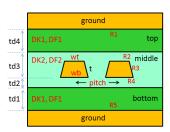
$$\varepsilon = \varepsilon_{\infty} + \Delta \varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10} \left( \frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f} \right)$$
$$= \varepsilon_r \cdot (1 - i \cdot \tan \delta)$$





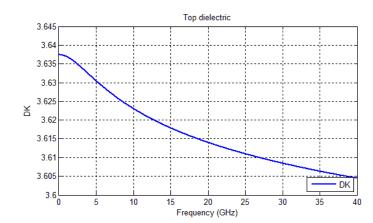


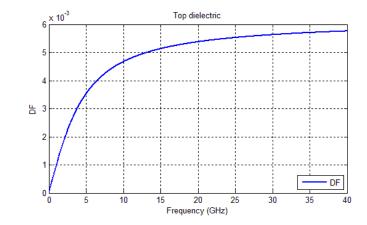
### Extracted DK2 and DF2 Model 3



 $\varepsilon_{\infty} = 3.46724$   $\Delta \varepsilon = 0.170196$  m1 = 9.58715m2 = 14.8352

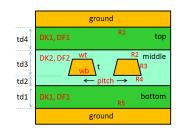
$$\varepsilon = \varepsilon_{\infty} + \Delta \varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10} \left( \frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f} \right)$$
$$= \varepsilon_r \cdot (1 - i \cdot \tan \delta)$$



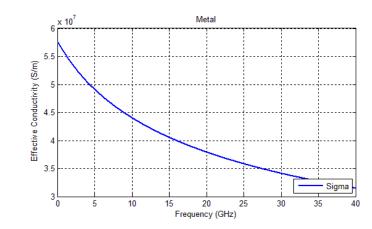




### **Extracted effective conductivity** *Model 3*

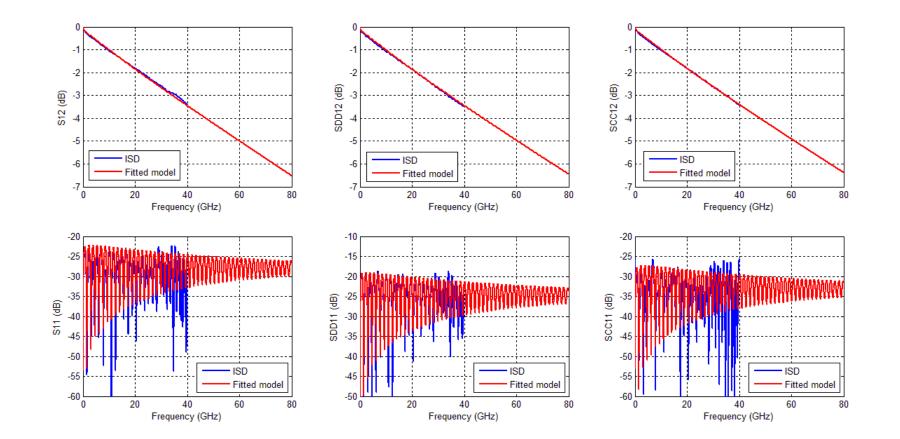


 $\sigma = 5.8 \times 10^7 \text{ S/m}$  $R_q = 0.324321 \,\mu\text{m}$ 





# Length- and frequency-scalable models can now be created.



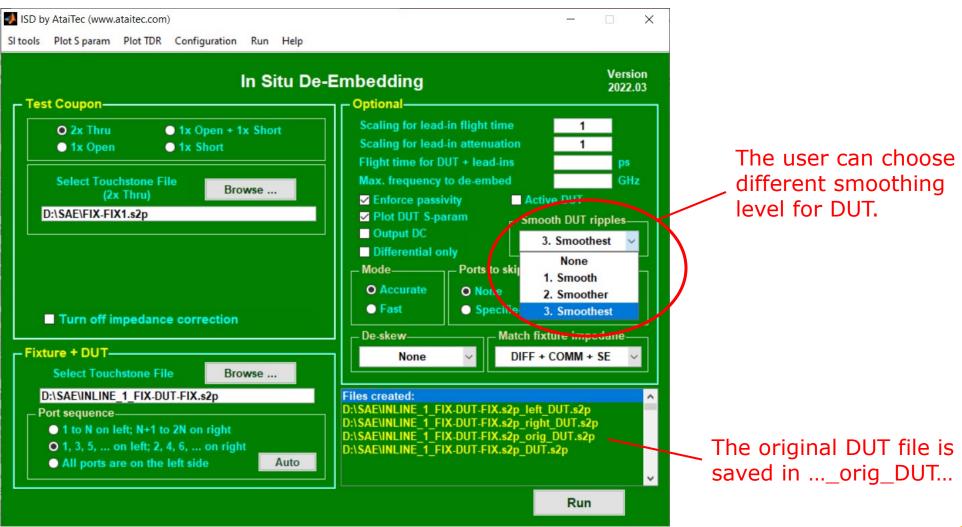


# New "Smoothing" feature improves accuracy for both raw measurement and de-embedded data

- S parameters can have artificial ripples
  - Before de-embedding
    - Due to bad calibration, port extension, bad contact or cable movement
  - After de-embedding
    - Due to 2x thru's IL and RL crossing each other or DUT much smaller than fixture
- New "Smoothing" feature lets the user remove such artificial ripples and improve data quality for both raw measurement and deembedded DUT data.
- Better correlation, compliance testing and measurement-based simulation can now be achieved as a result.



# "Smoothing" option





# **SAE/USCAR-49** inline connector example

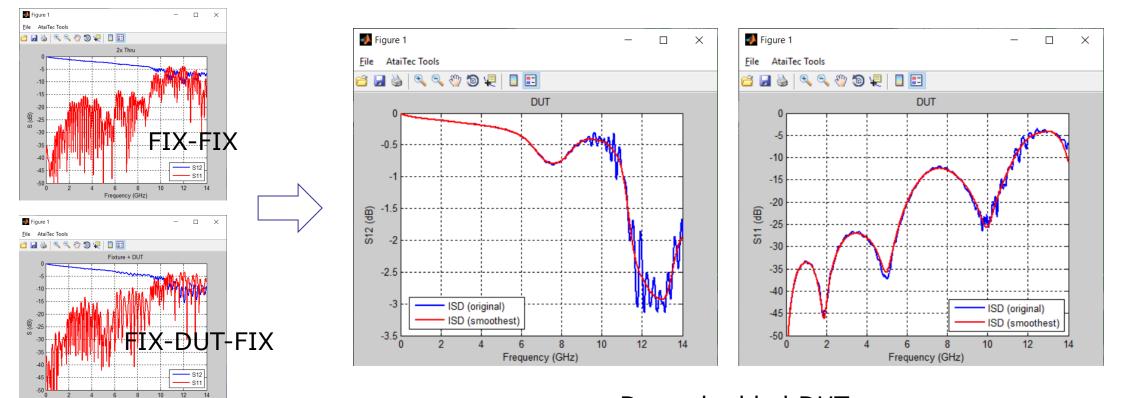
ISD gives smooth IL and RL across all frequencies.

6

250±10mm

Frequency (GHz)

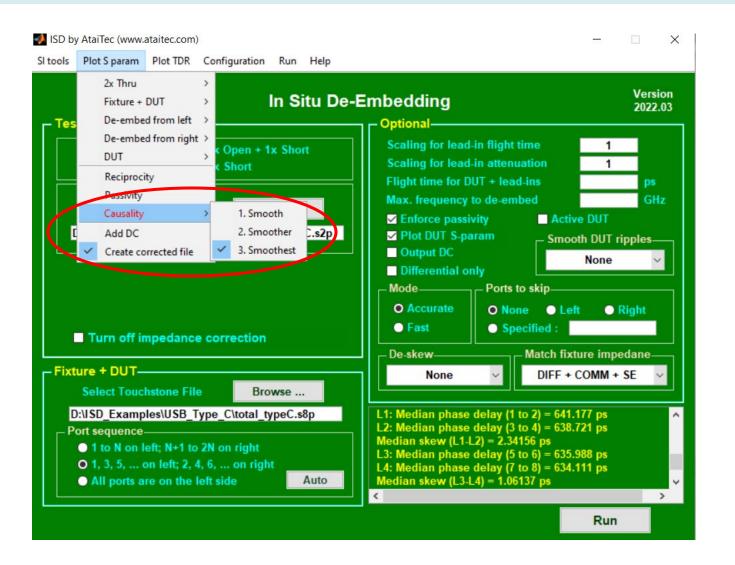
250±10mm



De-embedded DUT

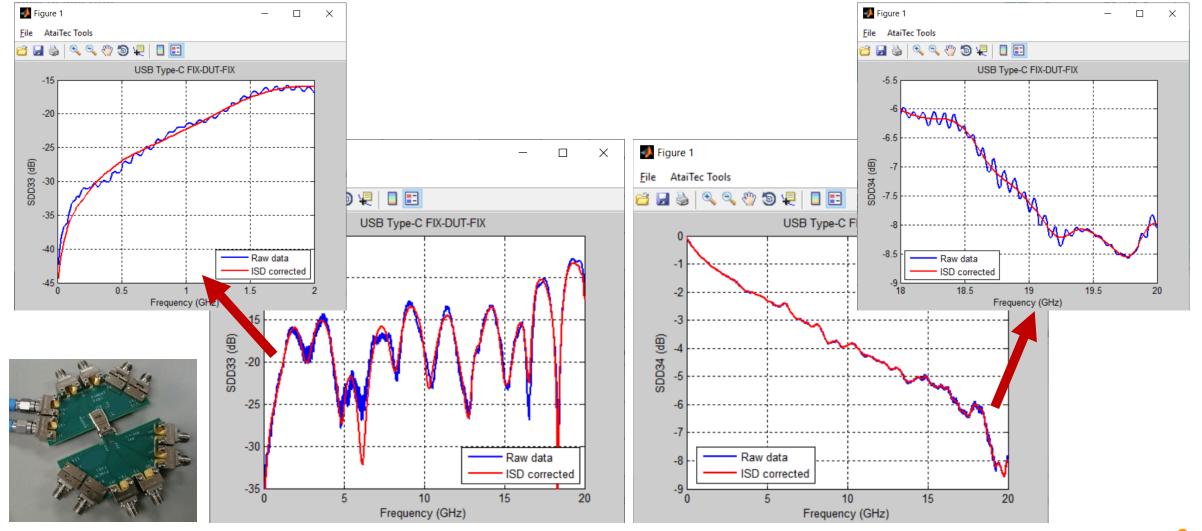


# Both raw measurement and de-embedded DUT data can also be corrected through "Plot S param->Causality..."





## **ISD corrects USB-C raw measurement in this example**



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## **PCIe CEM 5.0 spec. requires de-embedded results**

#### 6.3.6. Signal Integrity Requirements and Test Procedures for 32.0 GT/s Support

An electrical test fixture must be used for evaluating connector signal integrity. The test fixture effects are de-embedded from measurements. Test fixture requirements and recommendations are provided. Table 6.7 lines the electrical signal integrity parameters, requirements, and test procedures.

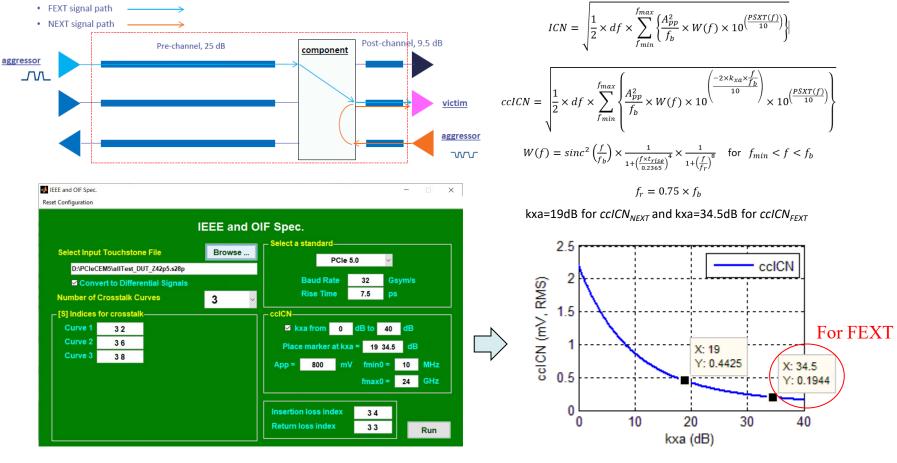
#### Table 6-7: Signal Integrity Requirements and Test Procedures for 32.0 GT/s Support

Parameter	Procedure	Requirements
Differential Insertion	EIA 364-101 The EIA standard shall be used with the following considerations:	[-0.1 - 0.05625 *f] dB up to 16 GHz;
Loss (DDIL)	<ol> <li>The measured differential S parameter shall be referenced to an 85 Ω differential impedance.</li> </ol>	[3 – 0.25*f] dB for
	<ol> <li>2. The test fixture shall meet the test fixture requirement defined in Section 6.3.5.1.</li> <li>3. The test fixture effect shall be removed from the measured S parameters. See Note 1.</li> </ol>	16 < f < 24 GHz
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations:	[-20 + 0.625*f] dB up to 16 GHz;
	<ol> <li>The measured differential S parameter shall be referenced to an 85 Ω differential impedance.</li> </ol>	[-24 + 0.875*f] dB for
	<ol> <li>The test fixture shall meet the test fixture requirement in Section 6.3.5.1.</li> <li>The test fixture effect shall be removed. See Note 1.</li> </ol>	16 < f < 24 GHz
Intra-pair Skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max
Differential	EIA 364-90	[1.5*f - 60] dB up to 10 GHz;
Near End Crosstalk (DDNEXT)	The EIA standard must be used with the following considerations: 1. The near end crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite	[(5/6)*f – 53.33] dB for 10 < f < 24 GHz;
	<ul> <li>sides of the connector, as listed in Table 6-6.</li> <li>2. This is a differential crosstalk requirement between a victim differential signal pair and all its adjacent differential signal pairs. The measured differential S parameter shall be referenced to an 85 Ω differential impedance.</li> <li>3. If this requirement is not met, ccICNnext can be used to determine the crosstalk energy in the given frequency band using Equation 1.</li> </ul>	cclCNnext for fmax = 24 GHz < 250 μV



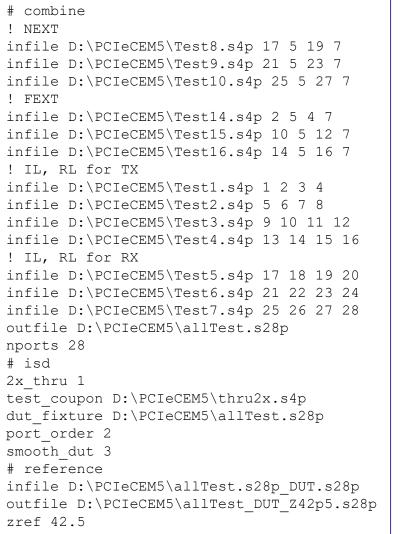
# **ISD accurately extracts pair-to-pair NEXT and FEXT for ccICN compliance testing**

ccICN: Component Contribution Integrated Crosstalk Noise

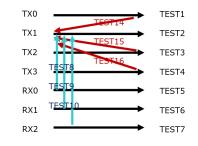


Import ISD results into ADK

# Automated batch file (1)



#### Combine multiple .s4p files into one .s28p file



#### Put IL, RL .s4p files last to have good IL, RL

#### Run ISD

Set "Smooth DUT ripples" to "Smoothest"

#### Change reference impedance



# Automated ISD batch file (2)

```
# adk "C:\Program Files (x86)\AtaiTec\ADK\adk2.exe"
# standard
infile D:\PCIeCEM5\allTest DUT Z42p5.s28p
spec no 7
differential 1
ccicn 1
il 34
rl 3 3
xtalk 3 2
xtalk 3 6
xtalk 3 8
figure tag ccICN FEXT
csv tag ccICN FEXT
# standard
infile D:\PCIeCEM5\allTest DUT Z42p5.s28p
spec no 7
differential 1
ccicn 1
il 3 4
rl 3 3
xtalk 3 9
xtalk 3 11
xtalk 3 13
figure tag ccICN NEXT
csv tag ccICN NEXT
```

#### Make all ADK functions available (License req'd)

Run PCIe 5.0 standard to get ccICN, etc.





# Summary

- Accurate de-embedding is crucial for design verification, compliance testing and PCB material property (DK, DF, roughness) extraction.
- Traditional de-embedding methods can give non-causal errors in device-under-test (DUT) results if the test fixture and calibration structure have different impedance.
- In-Situ De-embedding (ISD), with numerous advanced features beyond simply "splitting 2x thru", addresses such impedance difference through software instead of hardware, thereby improving de-embedding accuracy while reducing hardware cost.



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