In-Situ De-embedding (ISD)

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April 6, 2022

Fixture removal has come a long way

ISD

Impedance corrected de-embedding
Adjust for impedance variation between fixture and cal structure
Remove causality error in DUT results
2x thru or 1x open/short de-embedding
Arbitrary N-port de-embedding
Narrow-band de-embedding (for waveguide)
De-embed N ports from M ports (for devices)
De-embed via, socket or package
De-embed pair-to-pair crosstalk
De-embed mode conversion
Fixture has large impedance discontinuities
Fixture is much larger than DUT

TRL

2x thru

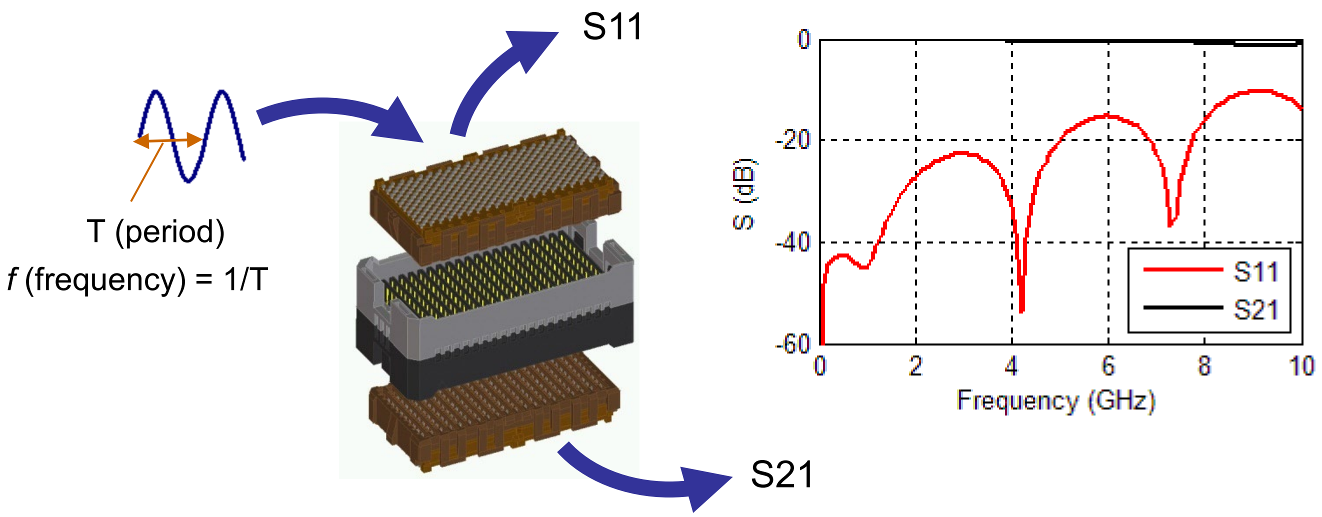
Port Extension

Outline

- What is causality
- What is In-Situ De-embedding (ISD)
- Comparison of ISD results with simulation and other tools
- How non-causal de-embedding affects connector compliance testing
- How to extract accurate PCB trace attenuation that is free of spikes and glitches
- How to extract a PCB's material property (DK, DF, roughness) by matching all IL, RL, NEXT, FEXT and TDR/TDT of de-embedded PCB traces
- New “Smoothing” feature for better accuracy to higher frequencies
- Automated PCIe 5.0 and ccICN compliance testing

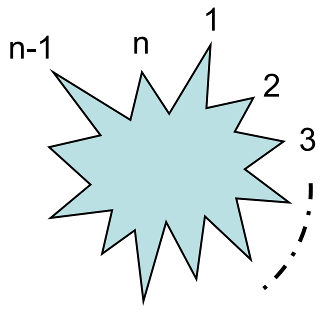
VNA and S parameter

- Vector network analyzer (VNA) is an equipment that launches a sinusoidal waveform into a structure, varies the period (or frequency) of waveform, and lets us observe the transmitted and reflected wave as “frequency-domain response”.
- Such frequency-domain response, when normalized to the incident wave, is called scattering parameter (or, S parameter).



What is S parameter

- For an n-port (or I/O) device, S parameter is an n x n matrix:



$$[S_{ij}]_{n\times n} = \begin{bmatrix} S_{11} & S_{12} & S_{13} & \dots & S_{1n} \\ S_{21} & S_{22} & S_{23} & \dots & S_{2n} \\ : & : & : & & : \\ S_{n1} & S_{n2} & S_{n3} & \dots & S_{nn} \end{bmatrix}$$

- Sij is called the S parameter from Port j to Port i.
- Sij has a unique property that its magnitude is less than or equal to 1 (or, 0 dB) for a passive device.

$$|S_{ij}| \le 1$$

$$S_{ij}(dB) = 20 \times \log_{10}|S_{ij}| \le 0 \ \ dB$$

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What is a Touchstone (.sNp) file

- S parameter at each frequency is expressed in Touchstone file format.

in GHz

S param

in dB and phase angle

Reference impedance

```
! Total number of ports = 4
! Total number of frequency points = 800
# GHZ  S  DB  R  50
0.025  -36.59296  48.77486  -41.40676  79.91354  -0.08648679  -6.544144  -49.50045  -105.618
       -41.39364  79.94686  -36.35592  51.52433  -49.4886  -105.5124  -0.09038406  -6.527076
       -0.08421237  -6.537903  -49.44814  -105.644  -36.0317  49.60022  -41.37105  79.91856
       -49.44393  -105.8186  -0.09834136  -6.542909  -41.36758  79.9318  -36.05645  48.98348
0.05  -32.22576  48.03161  -35.59394  74.15976  -0.1277169  -12.82876  -43.90183  -112.0995
       -35.58736  74.16304  -32.12694  50.92389  -43.90926  -112.0764  -0.132402  -12.7985
       -0.1242117  -12.82302  -43.89  -112.0248  -32.10987  50.3115  -35.56998  74.078
       -43.88424  -112.0517  -0.1381616  -12.80199  -35.56758  74.06782  -31.94136  50.49276
0.075  -29.88861  42.02766  -32.19713  68.06704  -0.1589249  -19.05252  -40.67476  -118.8188
       -32.19116  68.0941  -29.7086  45.41557  -40.63857  -118.837  -0.1635606  -19.01593
       -0.1603356  -19.0376  -40.63557  -118.8543  -29.89064  47.63852  -32.16917  67.94677
       -40.65711  -118.8021  -0.1737256  -19.02956  -32.16865  67.93389  -29.65444  46.15548

   :        :         :
```

Frequency in GHz

S11, S12, …, S44 in dB and phase angle

What is causality

cau·sal·i·ty
/kôˈzalədē/

noun

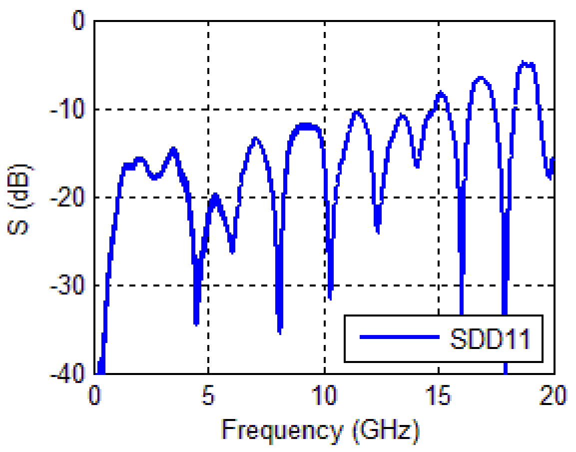
1. the relationship between cause and effect.
2. the principle that everything has a cause.

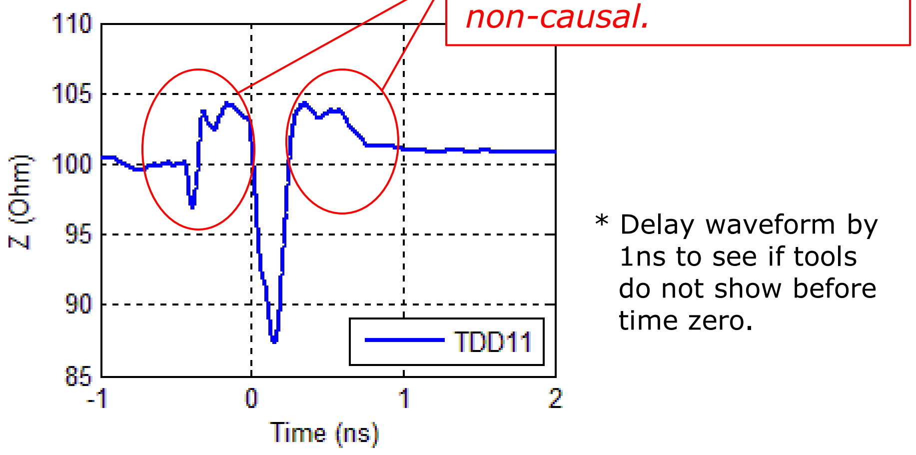
In other words:

Can not get something from nothing.

How to identify non-causal S parameter

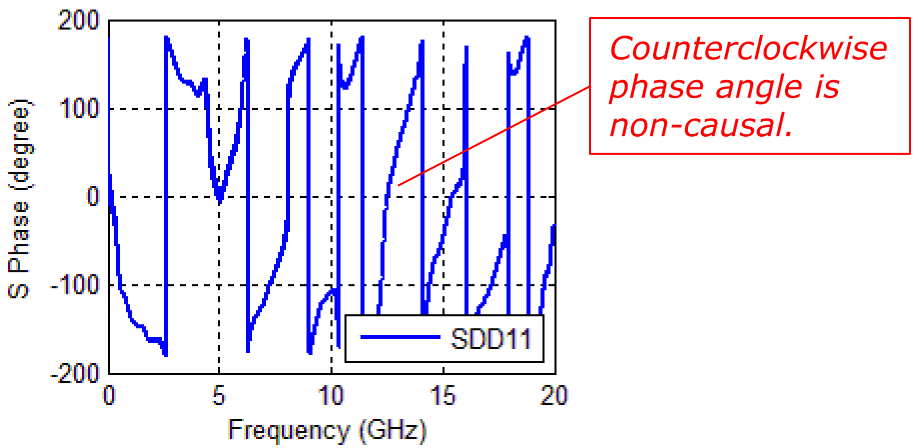
- Convert S parameter into TDR/TDT.





* Delay waveform by 1ns to see if tools do not show before time zero.

- Check phase angle.



Why does S parameter violate causality

- Measurement error (de-embedding), simulation error (material property) and finite bandwidth of S parameter all contribute to non-causality.
- Kramers-Kronig relations require that the real and imaginary parts of an analytic function be related to each other through Hilbert transform:

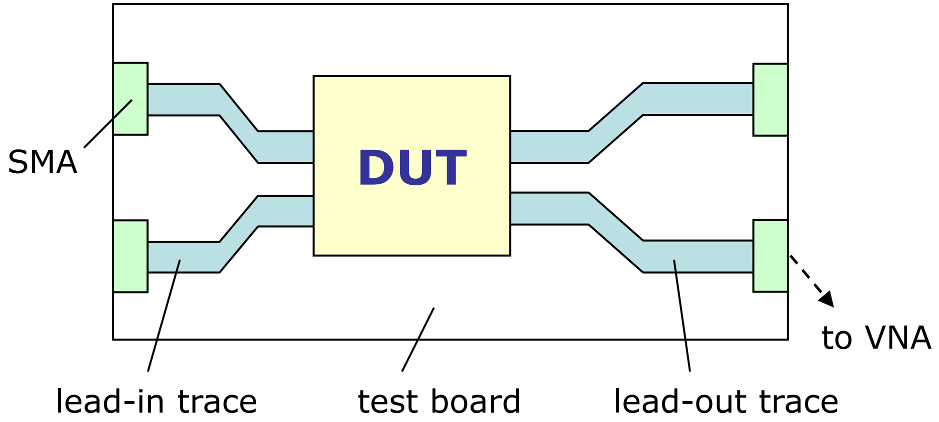
$$\Psi(\omega) = \Psi_R(\omega) + j\Psi_I(\omega)$$

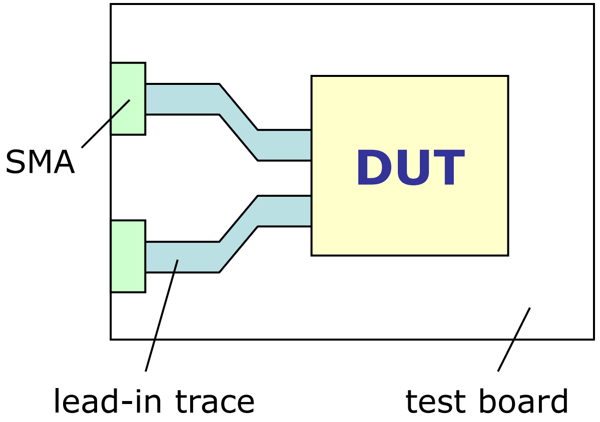
$$\Psi_R(\omega) = \frac{1}{\pi} P \int_{-\infty}^{\infty} \frac{\Psi_I(\omega')}{\omega' - \omega} d\omega'$$

$$\Psi_I(\omega) = -\frac{1}{\pi} P \int_{-\infty}^{\infty} \frac{\Psi_R(\omega')}{\omega' - \omega} d\omega'$$

What is de-embedding

- To remove the effect of fixture (SMA connector + lead-in/out) and extract the S parameter of DUT (device under test).

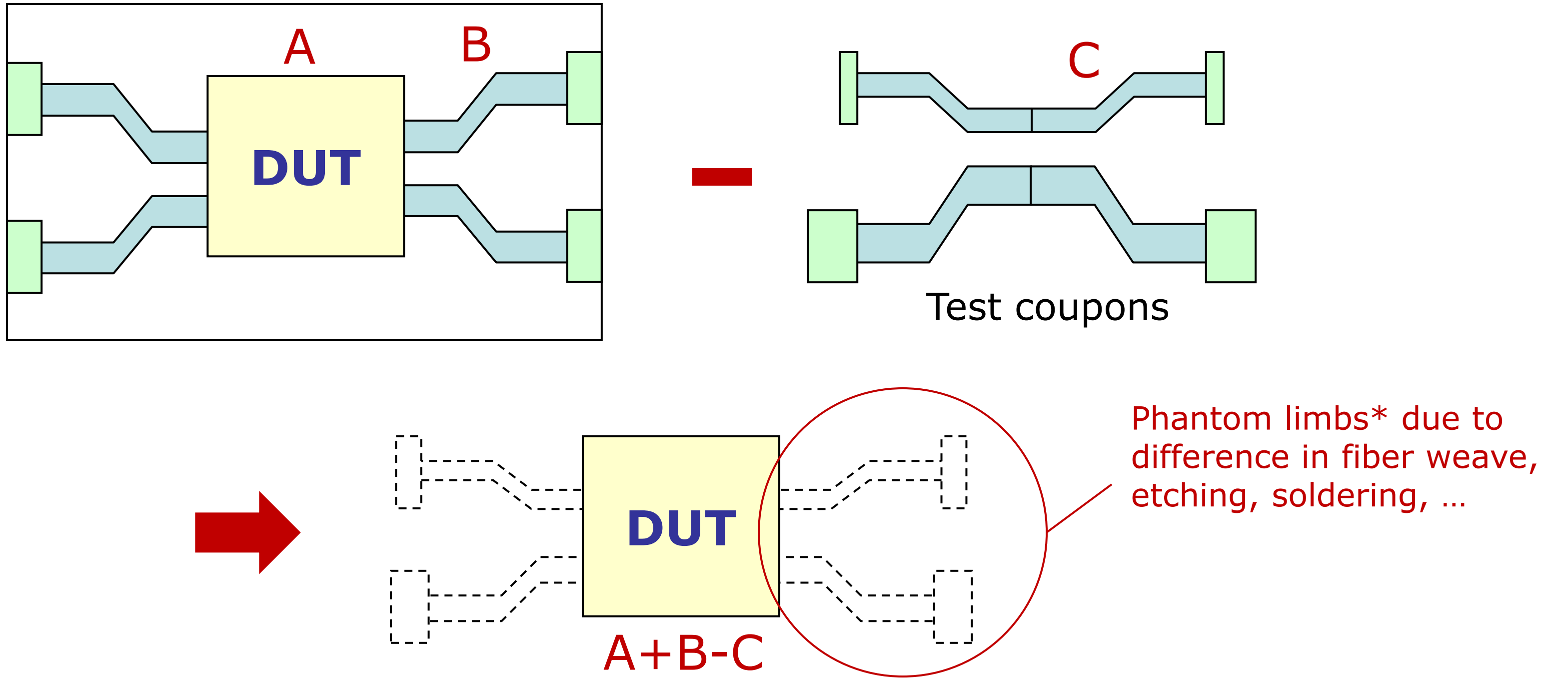




- The lead-ins and lead-outs don’t need to look the same.
- There may even be no lead-outs (e.g., package).

Why do most de-embedding tools give causality error

- Most tools use test coupons directly for de-embedding, so difference between actual fixture and test coupons gets piled up into DUT results.



* http://www.edn.com/electronics-blogs/test-voices/4438677/Software-tool-fixes-some-causality-violations by Eric Bogatin

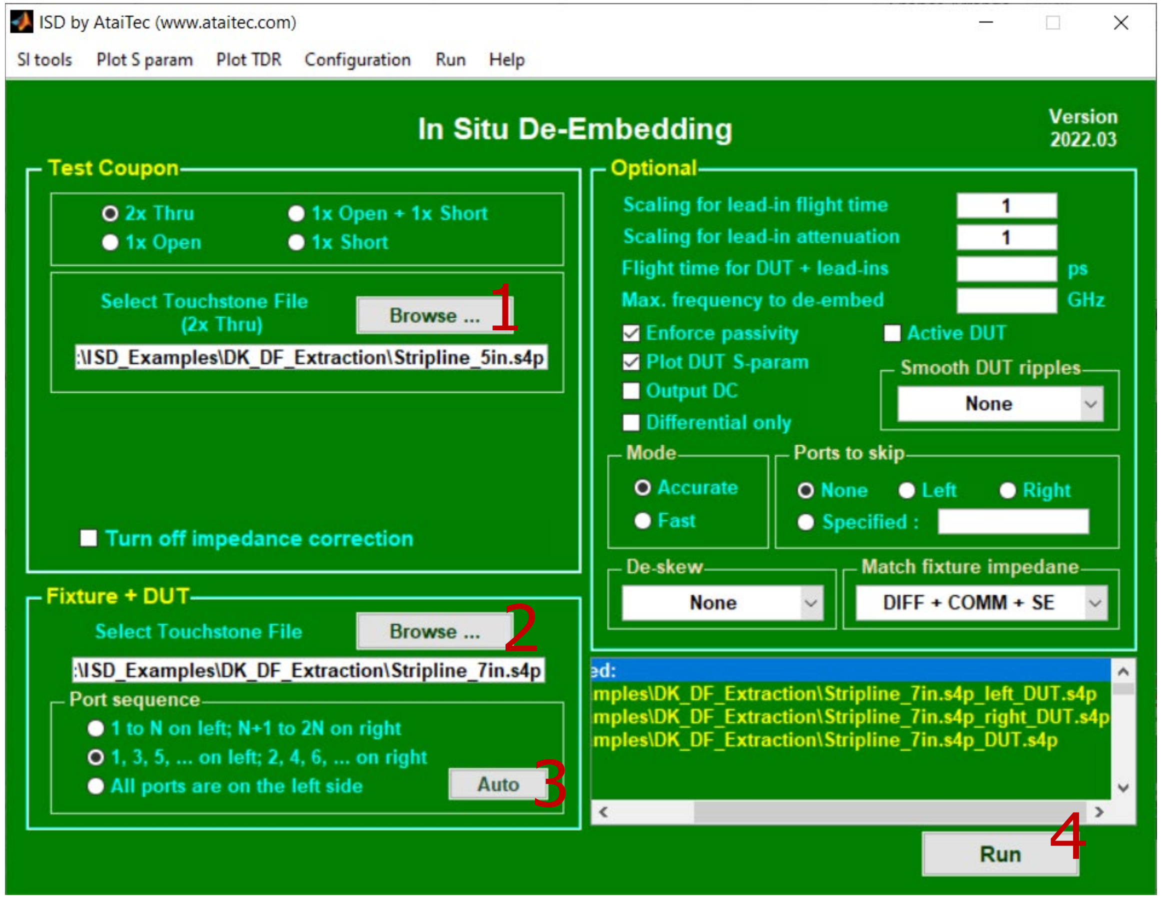
What is In-Situ De-embedding (ISD)

Introduced to address impedance variation

- ISD uses test coupon ("2x thru" or "1x open / 1x short") as reference and de-embeds fixture's actual impedance through numerical optimization.

- Other tools use test coupon directly for de-embedding and give causality error when test coupon and actual fixture have different impedance.

- ISD addresses impedance variation between test coupon and actual fixture through software, instead of hardware, improving de-embedding accuracy and reducing hardware cost.



ISD is integrated into R&S ZNA, ZNB

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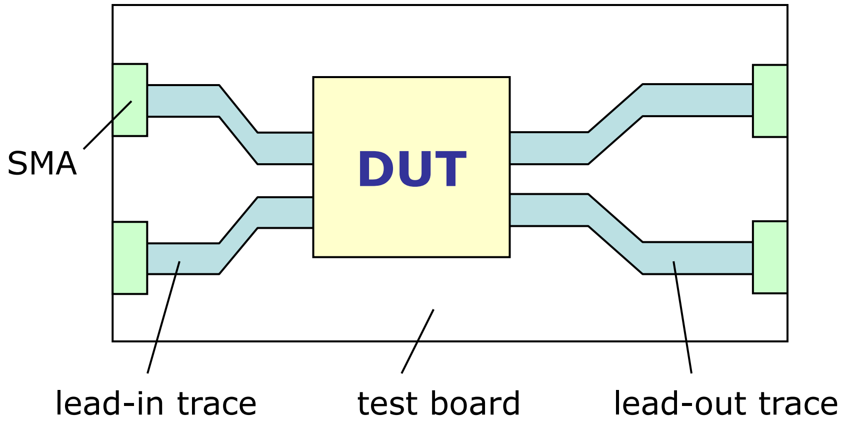
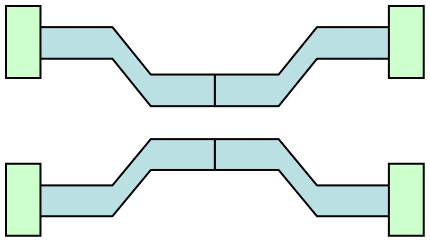
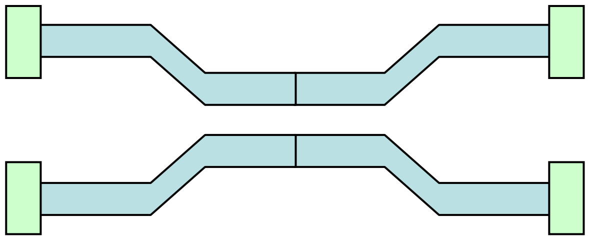
What is “2x thru”

- “2x thru” is 2x lead-ins or lead-outs.





2x thru for lead-ins

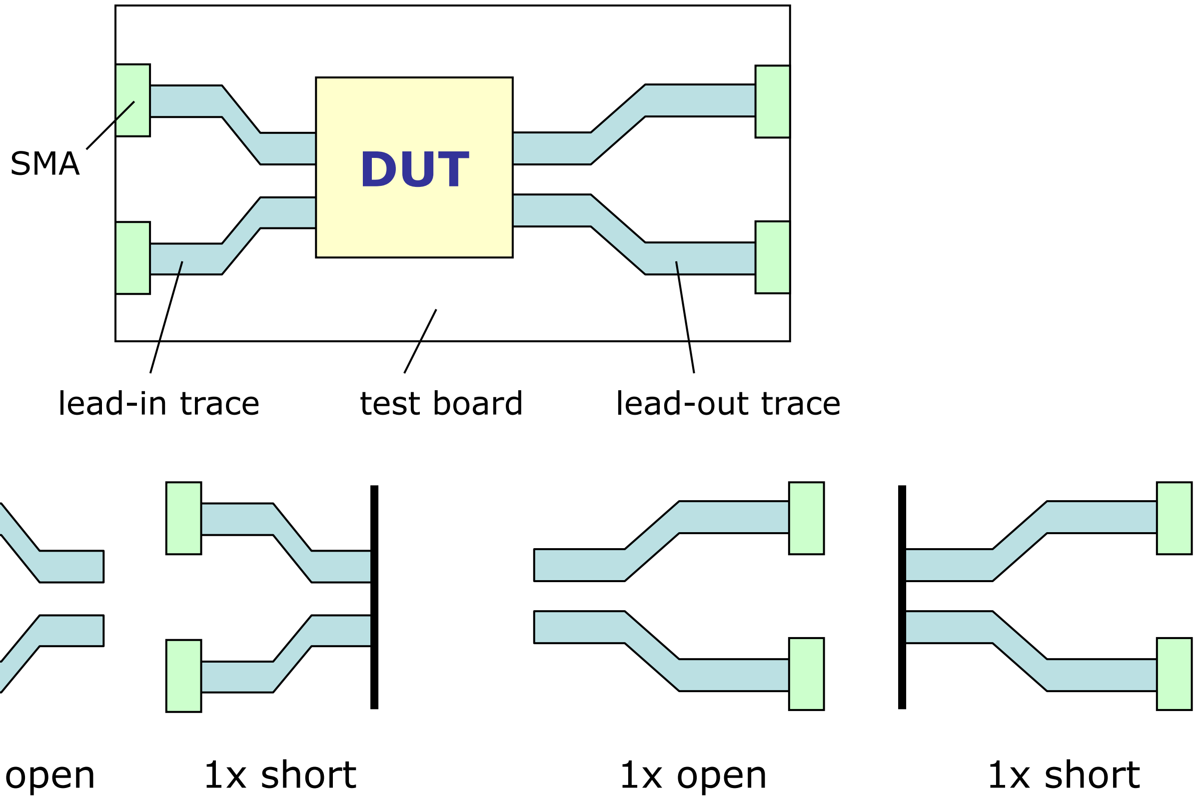


2x thru for lead-outs

2 sets of “2x thru” are required for asymmetric fixture.

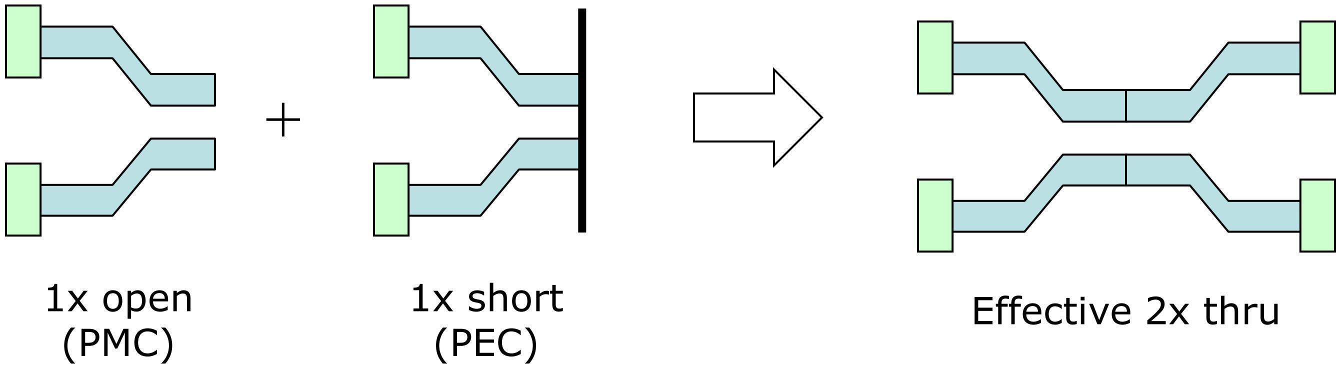
What is “1x open / 1x short”

- “1x open / 1x short” is useful when “2x thru” is not possible (e.g., connector vias, socket, package, …).



What is "1x open + 1x short"

- "1x open + 1x short" can be equated to effective* 2x thru.



$$[S]^{2x} = \begin{bmatrix} S_{11}^{2x} & S_{12}^{2x} \\ S_{12}^{2x} & S_{11}^{2x} \end{bmatrix} = \frac{1}{2} \begin{bmatrix} S_{11}^{open} + S_{11}^{short} & S_{11}^{open} - S_{11}^{short} \\ S_{11}^{open} - S_{11}^{short} & S_{11}^{open} + S_{11}^{short} \end{bmatrix}$$

* C.C. Huang, "Fixture de-embedding using calibration structures with open and short terminations," US patent no. 10761175B2, Sep. 1, 2020.

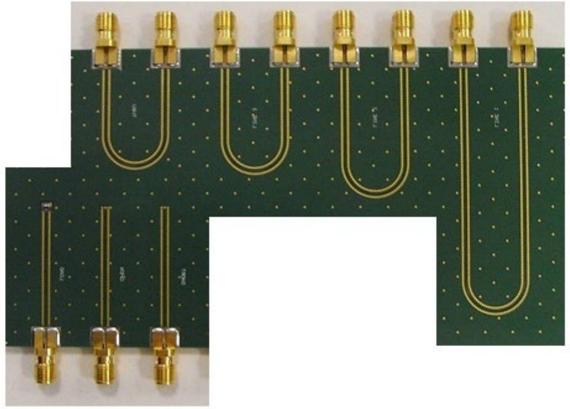
ISD advantages

	ISD	Others
Accuracy	Accurate and causal DUT results. Easier to correlate with simulation, improving design and time to market.	Artificial ripples in S-param; non-physical TDR/TDT before and after DUT. Difficult to correlate with simulation, resulting in long design cycle.
Cost saving	Saves hardware cost because inexpensive test fixtures with large impedance variation can be used.	Requires expensive test fixtures to tighten impedance variation.
	Precise qualification in meeting compliance spec. Avoid components from being thrown away by mistake.	Good components may fail compliance spec because of de-embedding error and get thrown away by mistake.
Technology	Uses impedance corrected 2x thru or 1x open/short to de-embed actual fixture impedance	Uses 2x thru or 1x open/short to directly de-embed fixture, resulting in causality error.
Capabilities	Able to de-embed arbitrary number of ports.	No
	Able to de-embed n ports from m-port structures (n<=m and n, m are arbitrary). Essential for RF and MEMS devices.	No
	Able to de-embed mode conversion	No
	Able to use single line to de-embed crosstalk	No
	Able to de-embed longer or shorter than existing test coupons	No
	Automatic de-skew	No
	Creates effective 2x thru from 1x open + 1x short	No
	Extracts small DUT from a large board	Error is extremely large if DUT is much smaller than test fixture.
	De-embeds asymmetric structures	Claims to be able to de-embed asymmetric structures but assumes IL to be identical on both left and right sides of test fixture.

* See https://ataitec.com/docs/ISD_advantages.pdf for a complete list.

Why ISD is more accurate and saves $$$

TRL calibration board



- More board space - Multiple test coupons are required.
- Test coupons are used directly for de-embedding.
- All difference between actual fixture and test coupons gets piled up into DUT results.
- Expensive SMAs, board materials (Roger) and tight-etching-tolerance are required.
  - Impossible to guarantee all SMAs and traces are identical (consider weaves, etching, …)
- Time-consuming manual calibration is required.
  - Reference plane is in front of DUT.

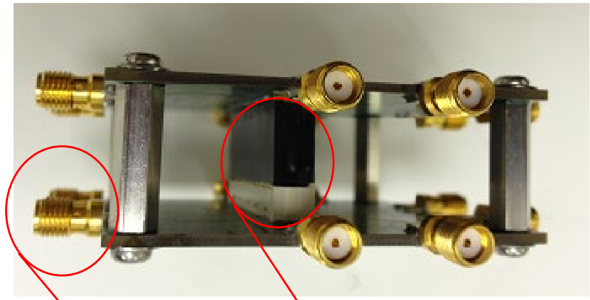
ISD test coupon

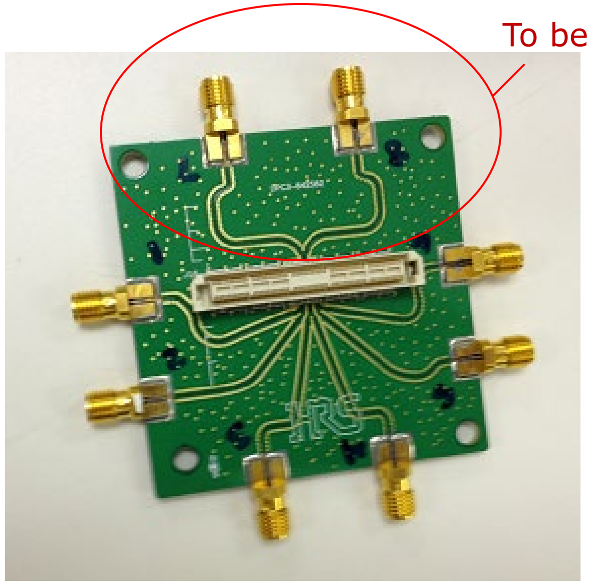
- Only one 2x thru test coupon is needed.
- Test coupon is used only for reference, not for direct de-embedding.
- Actual fixture impedance is de-embedded.
- Inexpensive SMAs, board materials (FR4) and loose-etching-tolerance can be used.
- ECal can be used for fast SOLT calibration.
  - Reference plane is in front of SMA.
  - De-embedding requires only two input files: 2x thru and DUT board (SMA-to-SMA) Touchstone files.
  - Both de-embedding and DUT files are provided as outputs.

* TRL = Thru-Reflect-Line

Example 1: Mezzanine connector
ISD vs. TRL

- In this example, we will use ISD and TRL to extract a mezzanine connector and compare their results.

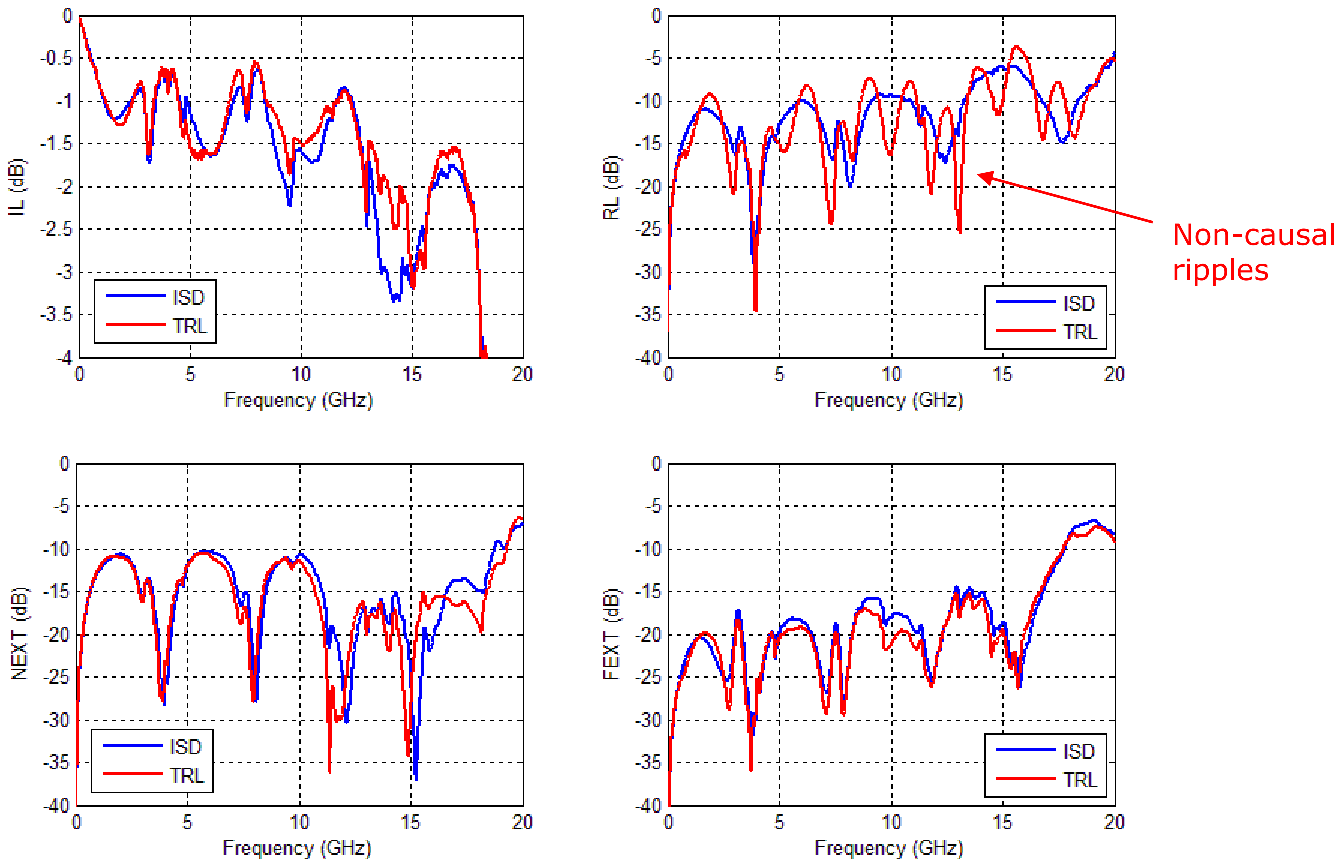




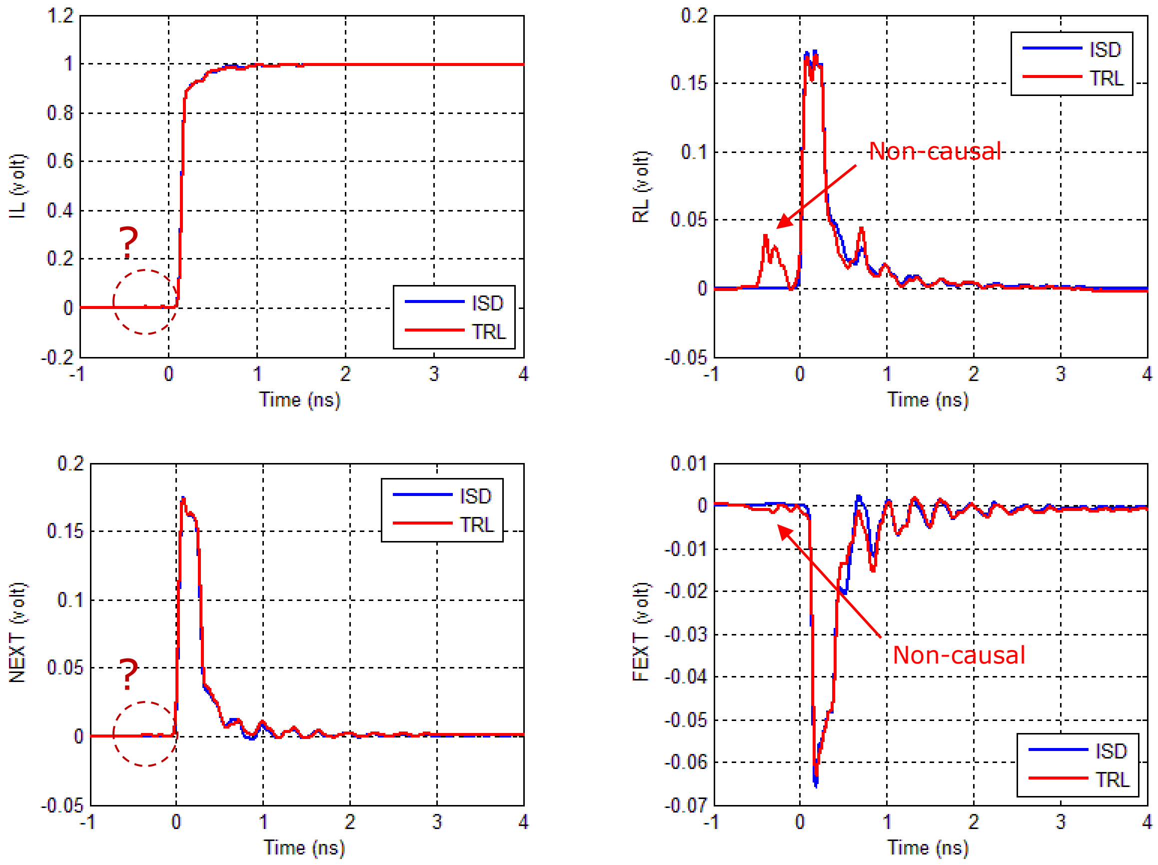
*Courtesy of Hirose Electric

DUT results after ISD and TRL
Which one is more accurate?

- TRL gives too many ripples in return loss (RL) for such a small DUT.



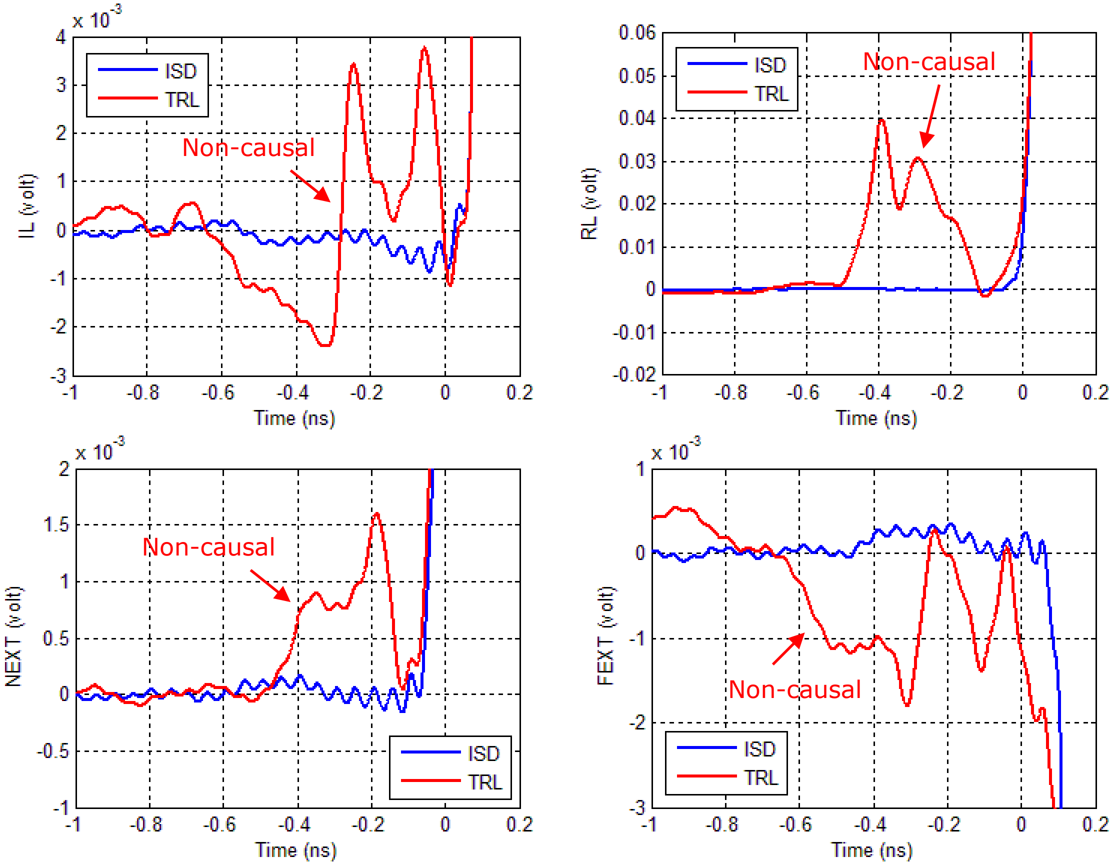
Converting S parameter into TDR/TDT shows non-causality in TRL results



Rise time = 40ps (20/80)

Zoom-in shows non-causal TRL results in all IL, RL, NEXT and FEXT

- TRL causes time-domain errors of 0.38% (IL), 25.81% (RL), 1.05% (NEXT) and 2.86% (FEXT) in this case*.

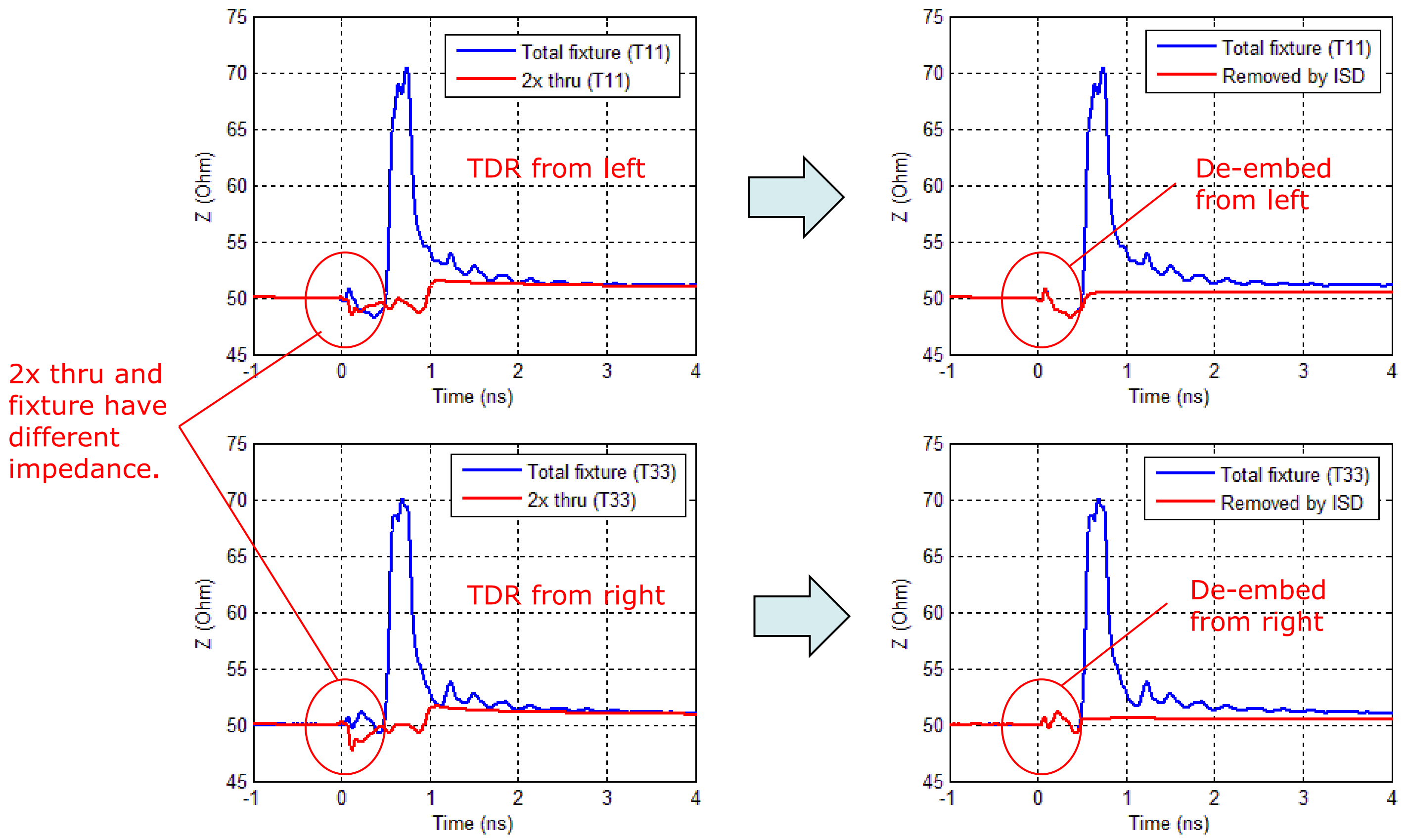


* The percentage is larger with single-bit response and/or faster rise time.

Rise time = 40ps (20/80)

How did ISD do it?

- Through numerical optimization, ISD de-embeds fixture’s impedance exactly, independent of 2x thru’s impedance.

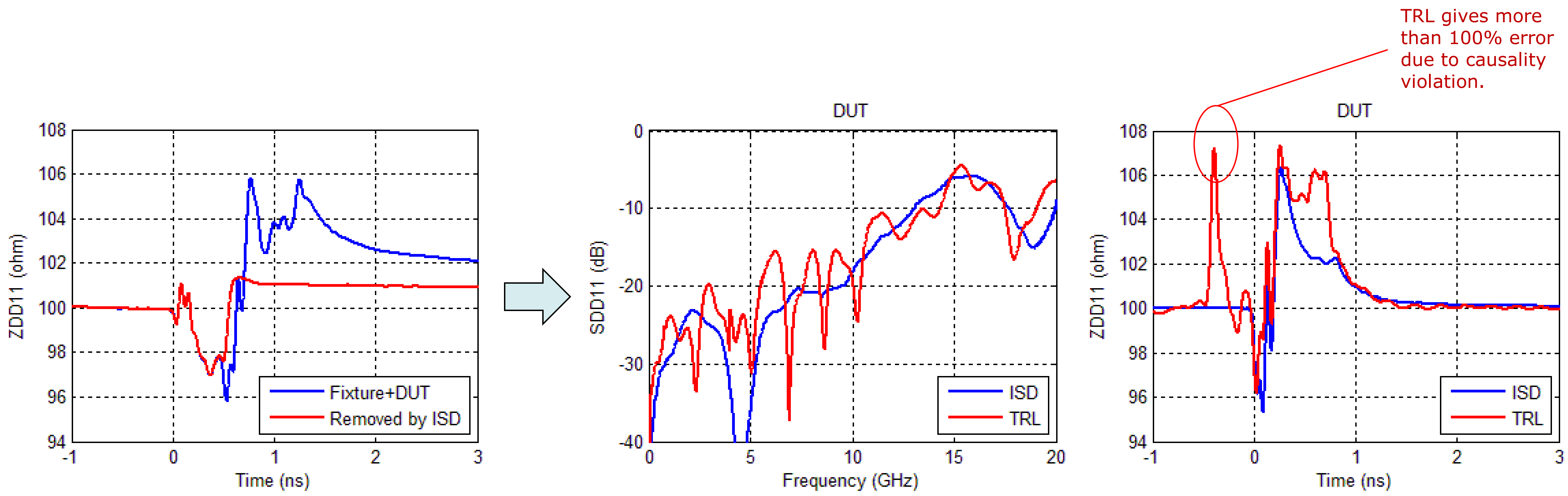


Rise time = 40ps (20/80)

TRL can give huge error in SDD11 even with less than 5% impedance variation*

* See previous slide.

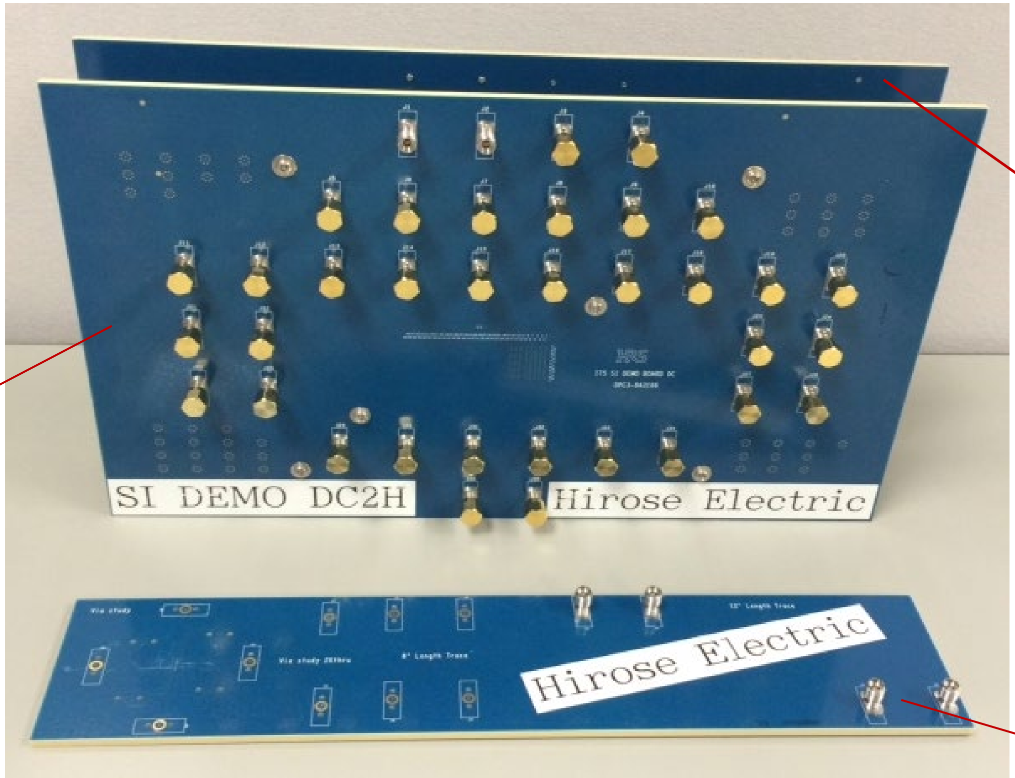
- ISD is able to de-embed fixture's differential impedance with only a single-trace 2x thru.



Rise time = 40ps (20/80)

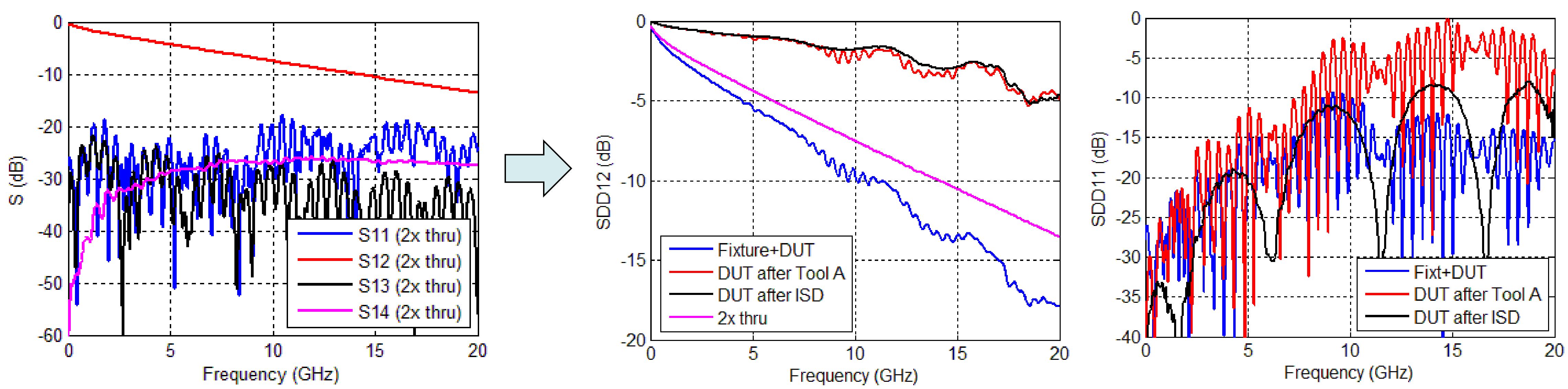
Example 2: Mezzanine connector
Extracting DUT from a large board

- TRL is impractical for de-embedding large and coupled lead-ins/outs.



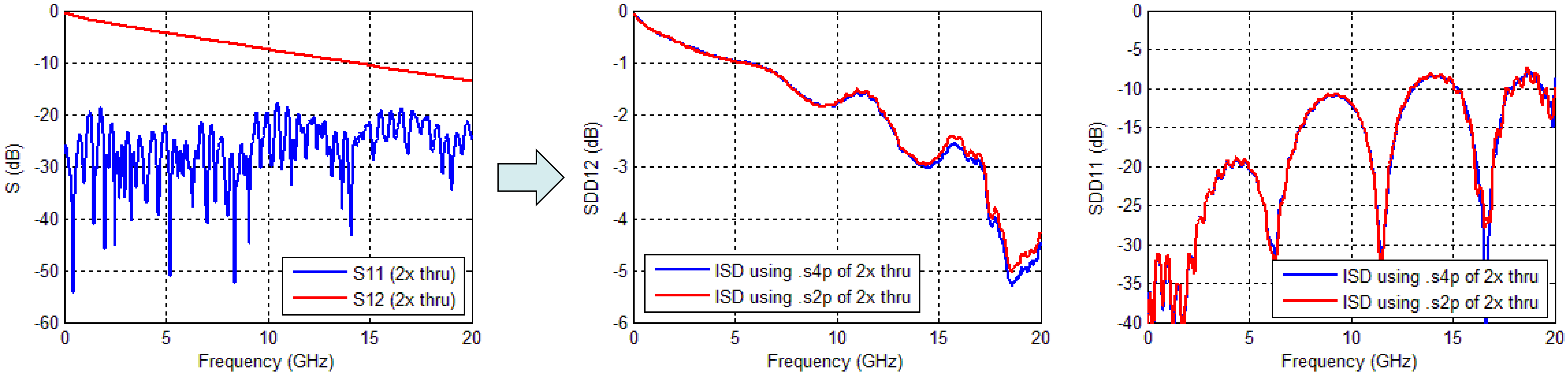
ISD can use a .s4p file of 2x thru for de-embedding

- TRL would have required many long and coupled traces.
- “Tool A” gave incorrect results.



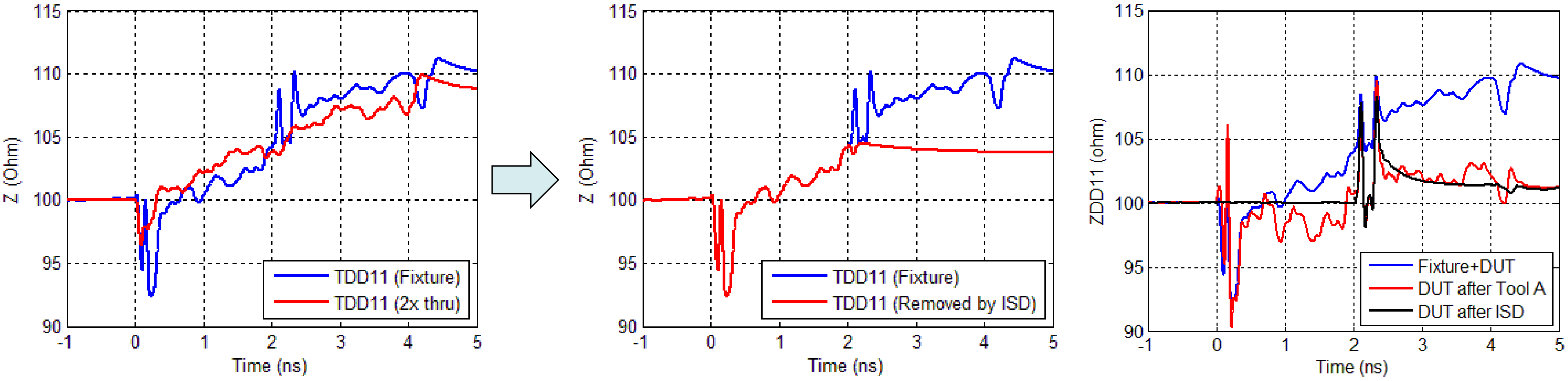
ISD can even use a .s2p file of 2x thru to de-embed crosstalk…

- And the results are similar!



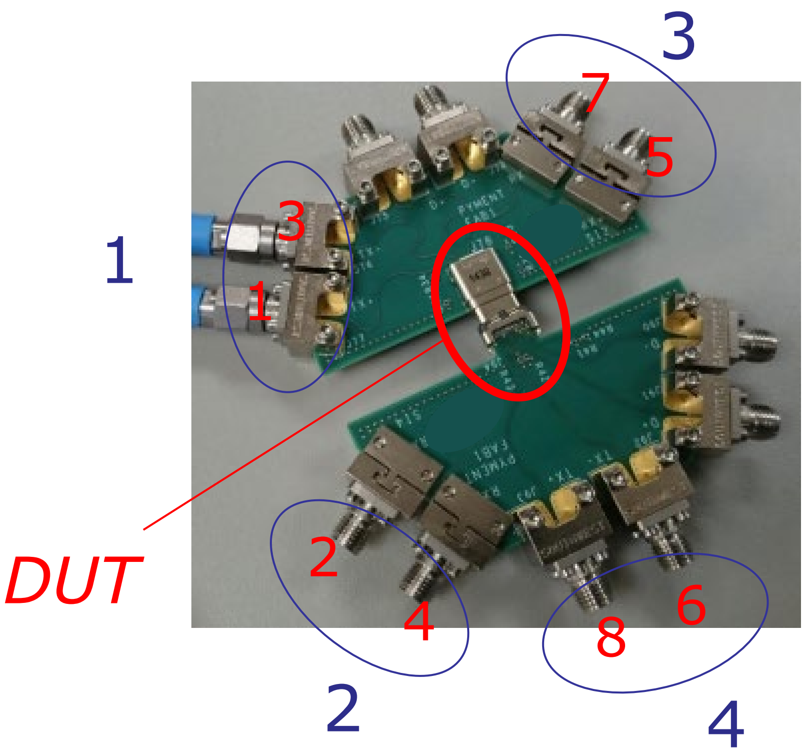
ISD allows a large demo board to double as a characterization board

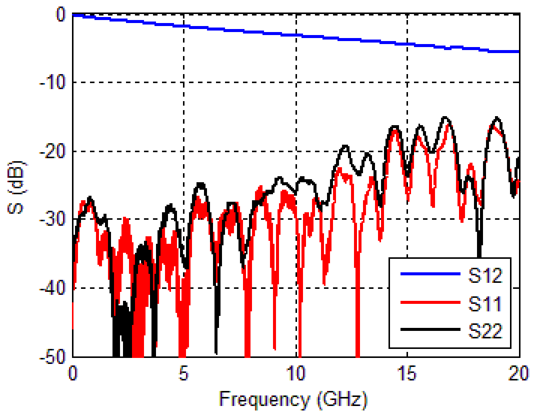
- ISD de-embeds fixture's impedance regardless of 2x thru's impedance.
- "Tool A" gave causality error before and after DUT.



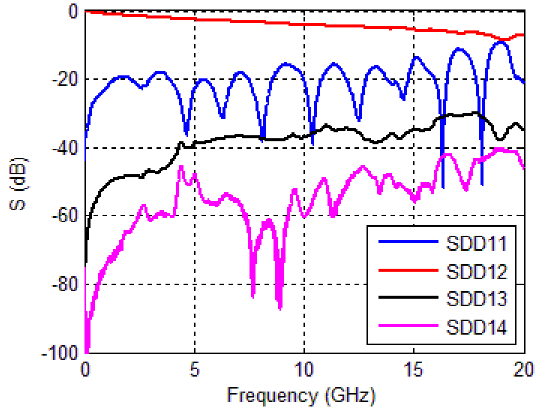
Example 3: USB type C mated connector
ISD vs. Tool A

- Good de-embedding is crucial for meeting compliance spec.





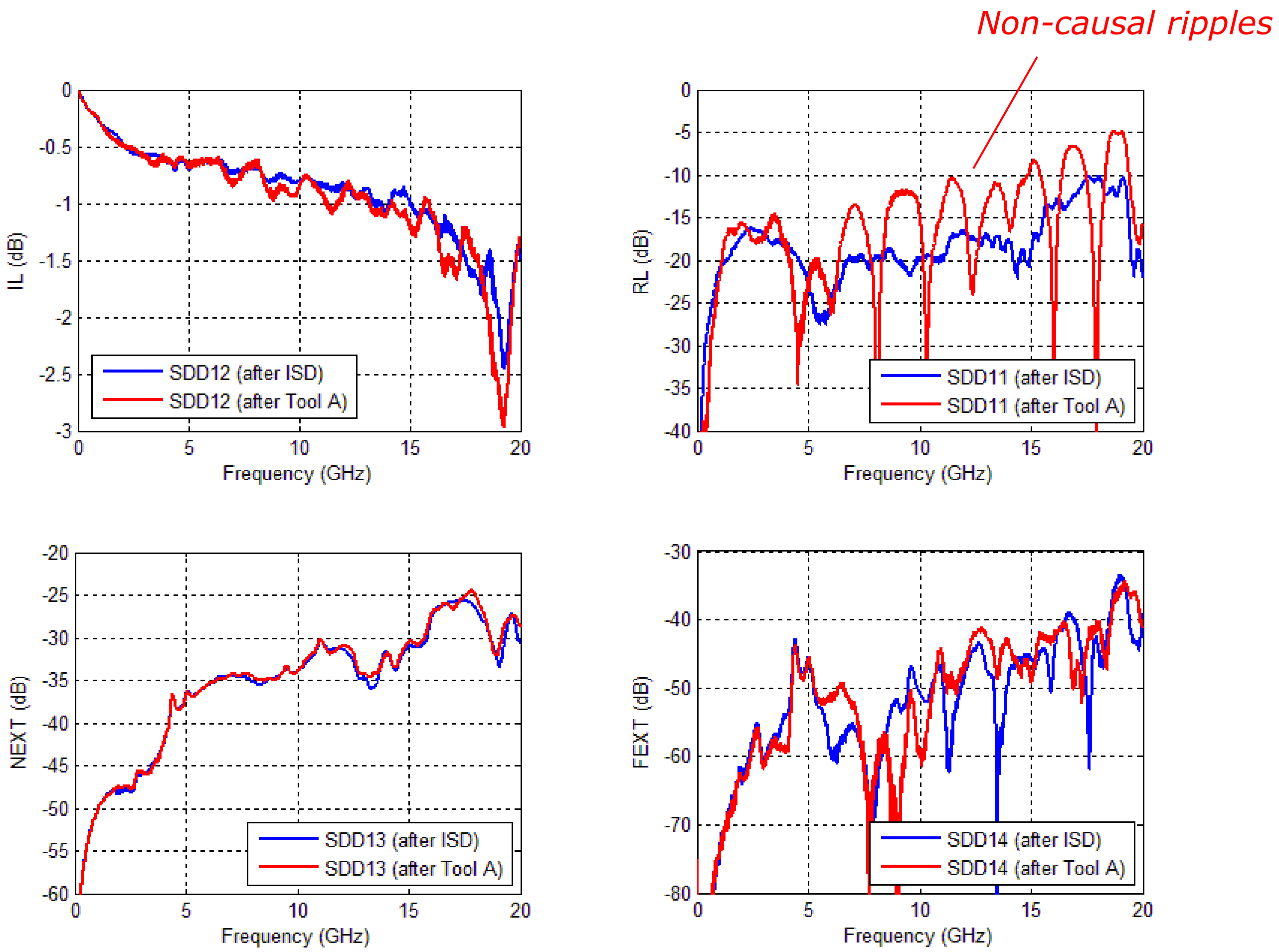
2x thru



Fixture

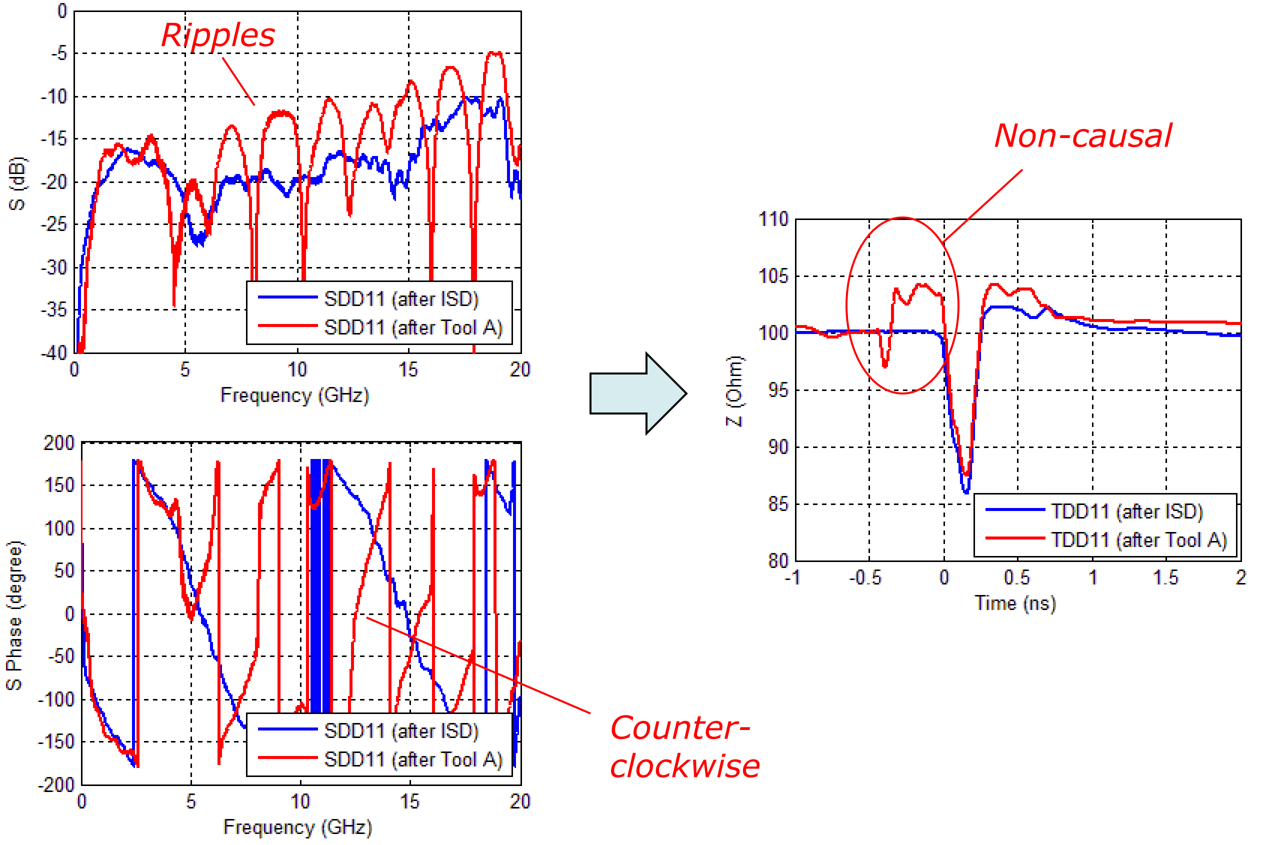
DUT results after ISD and Tool A
Which one is more accurate?

- “Tool A” gives too many ripples in return loss (RL) for such a small DUT.



Converting S parameter into TDR/TDT shows non-causality in Tool A results

- Counter-clockwise phase angle is another indication of non-causality.

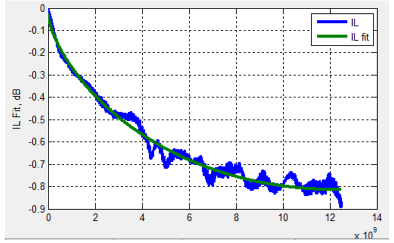


De-embedding affects pass or fail of compliance spec.

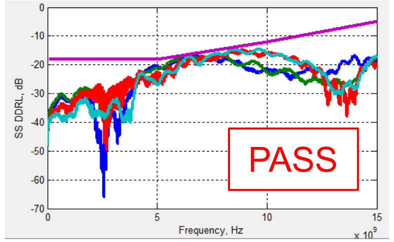
- ISD improves IMR and IRL (from compliance tool).

ISD

	Value (Pass/Fail)
ILfit@2.5GHz	-0.4
ILfit@5.0 GHz	-0.6
ILfit@10.0GHz	-0.8
IMR	-45.1
IRL	-23.2
INEXT	-41.5
IFEXT	-49.2
SCD12/SCD21	-23



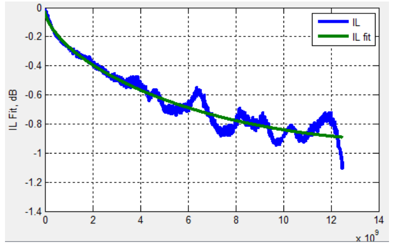
IL



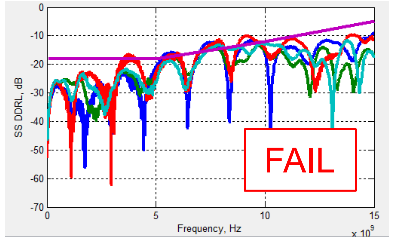
RL

Tool A

	Value (Pass/Fail)	Spec
ILfit@2.5GHz	-0.4	-0.6
ILfit@5.0 GHz	-0.6	-0.8
ILfit@10.0GHz	-0.9	-1.0
IMR	-43.7	-40
IRL	-20.8	-18
INEXT	-41.5	-44
IFEXT	-49.3	-44
SCD12/SCD21	-23.2	



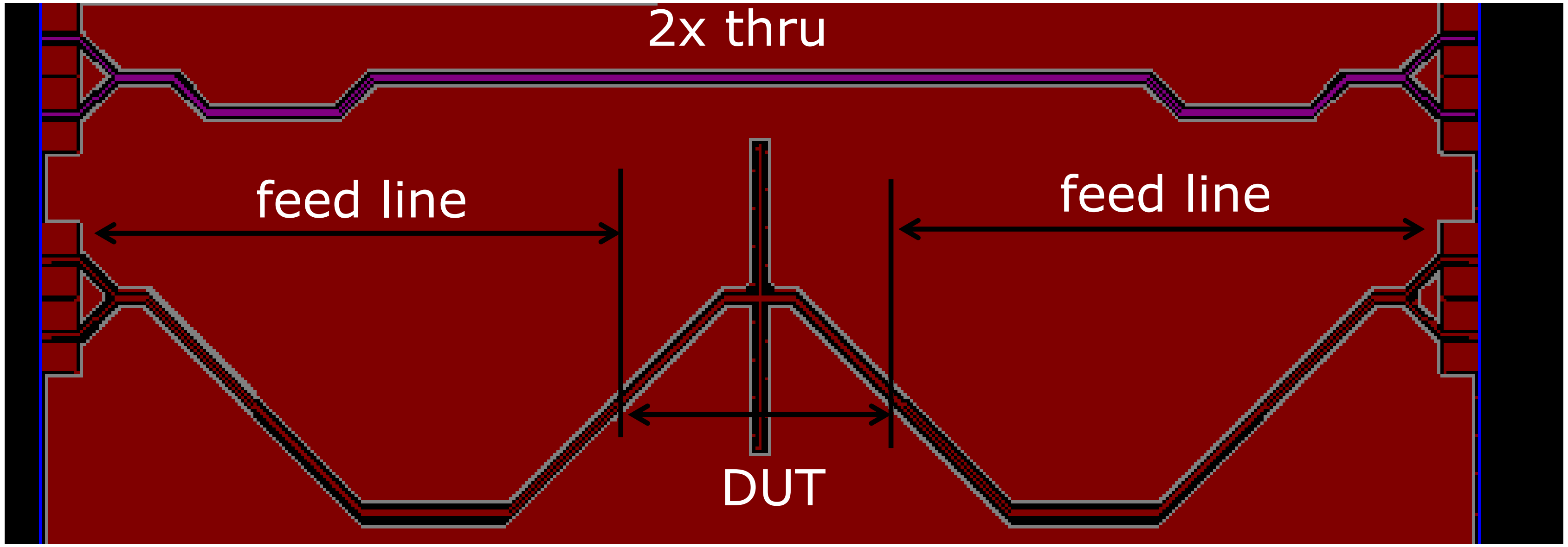
IL



RL

Example 4: Resonator
ISD vs. Tool A vs. simulation

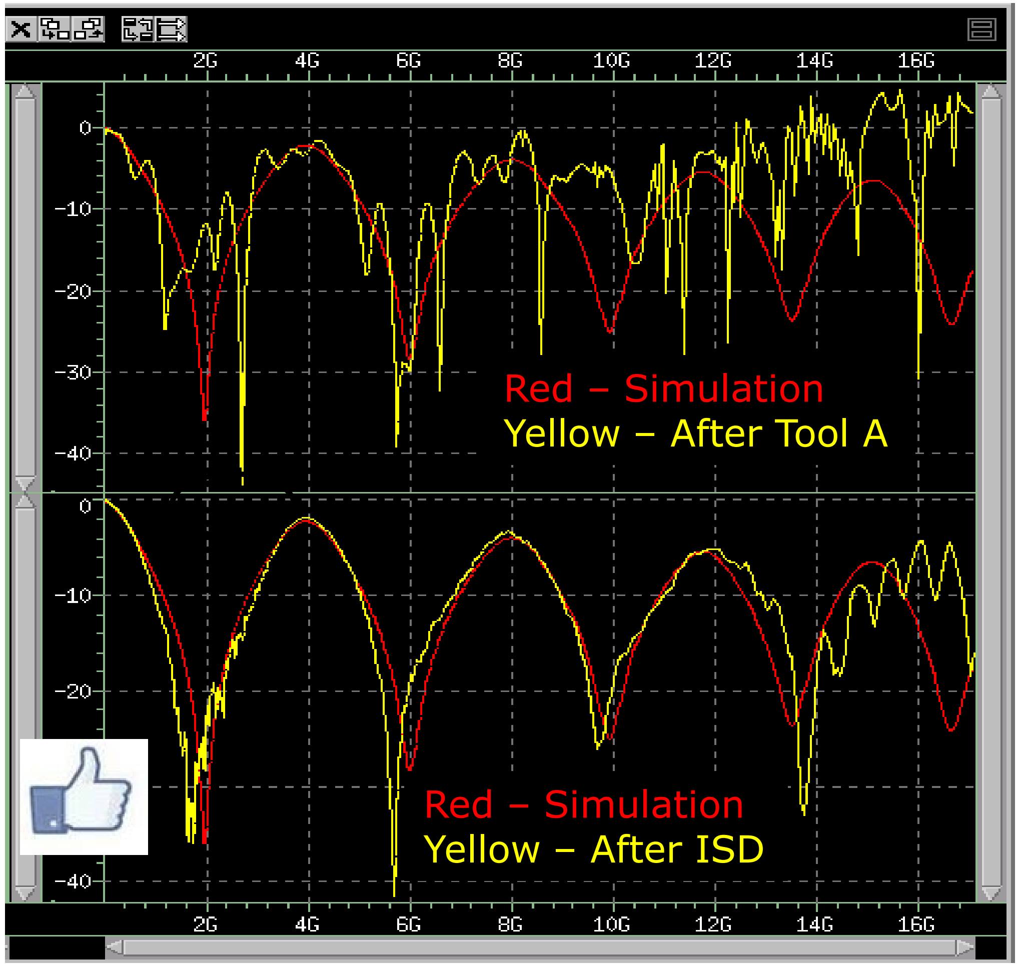
- Good de-embedding is crucial for design verification (i.e., correlation) and improvement.



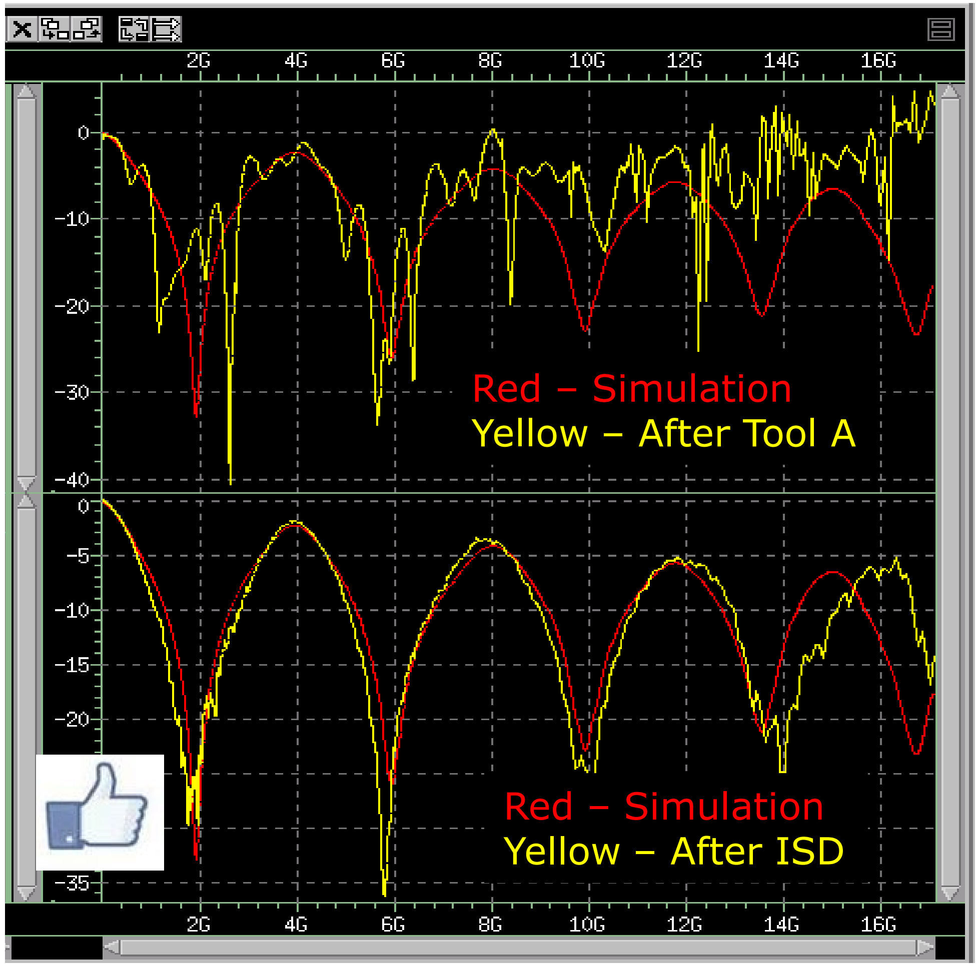
ISD correlates with simulation

Good correlation is crucial for design improvement

SDD11

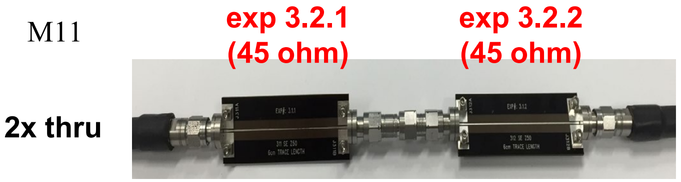


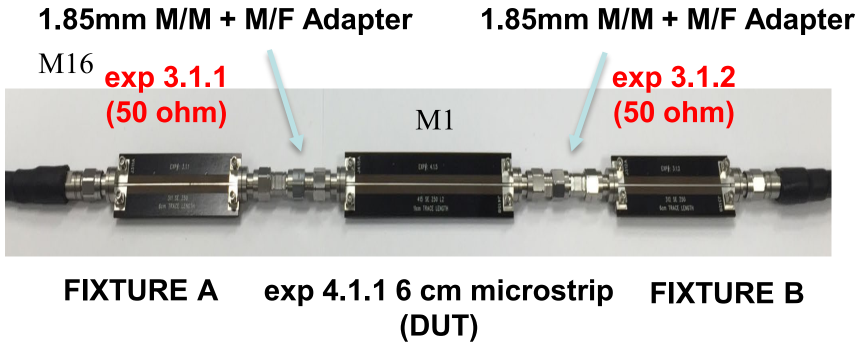
SCC11



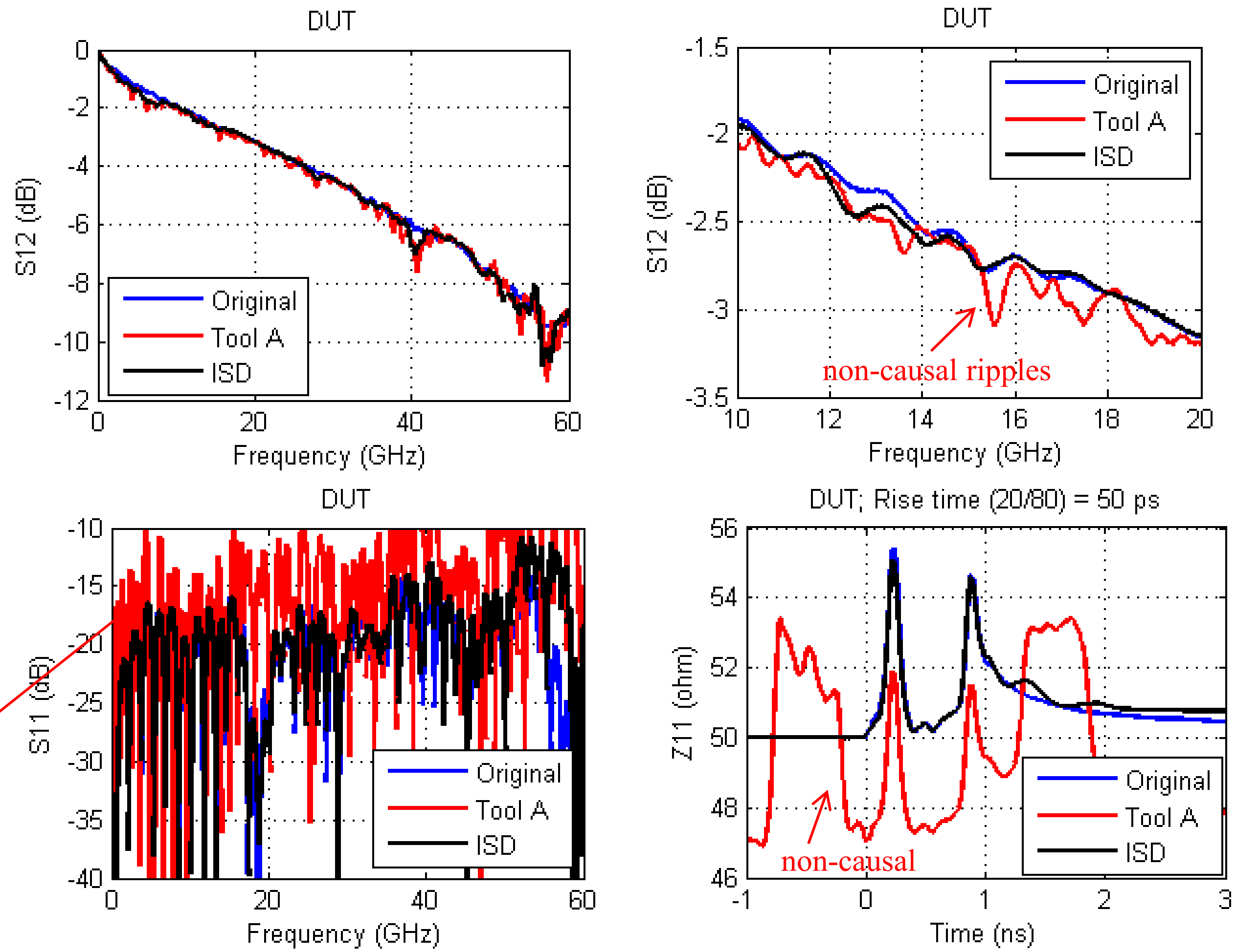
Example 5: IEEE P370 plug and play kit
*Using 45 ohm 2x thru to de-embed 50 ohm fixture**

* To mimic possible PCB impedance variation



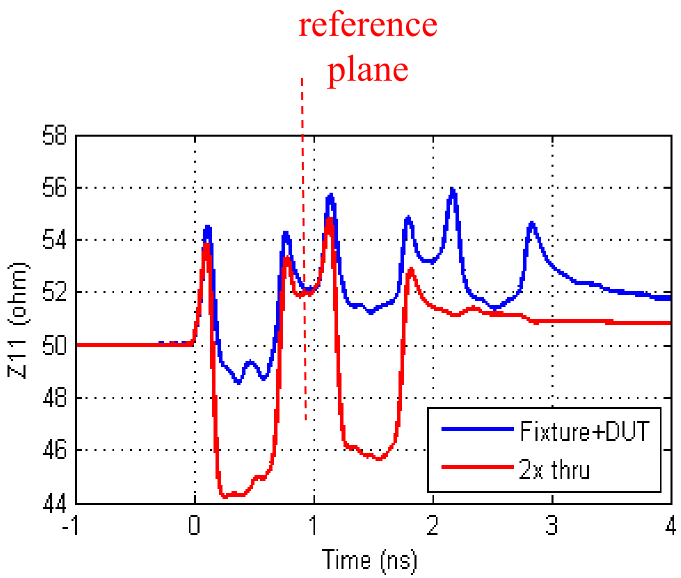


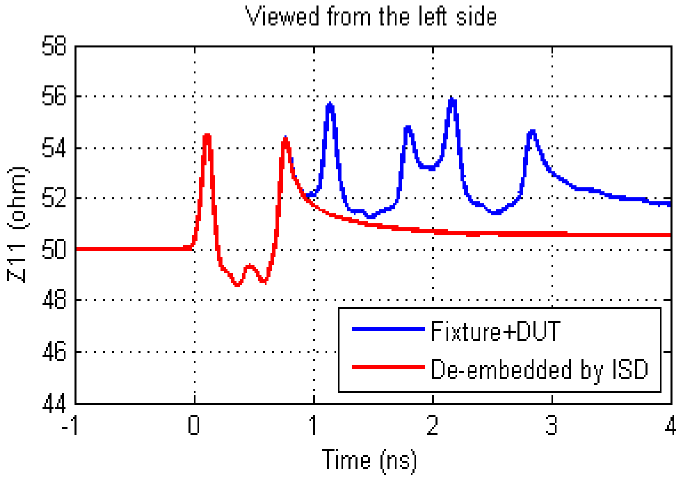
Inaccurate RL is not suitable for DK/DF/SR extraction.



2x thru vs. fixture impedance

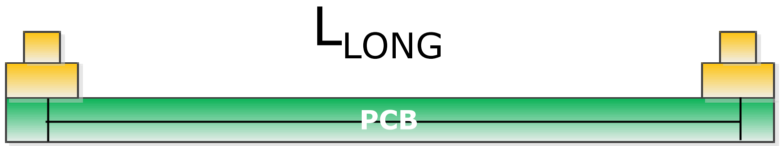
- ISD de-embeds fixture's impedance, not 2x thru's impedance.



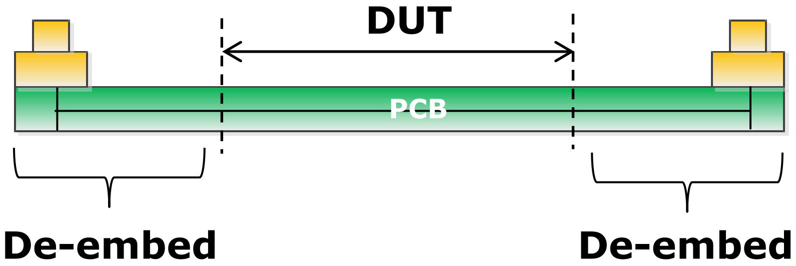


Example 6: PCB trace attenuation
ISD vs. eigenvalue (Delta-L)

- De-embed short trace (+ launch) from long trace (+ launch) to get trace-only attenuation.

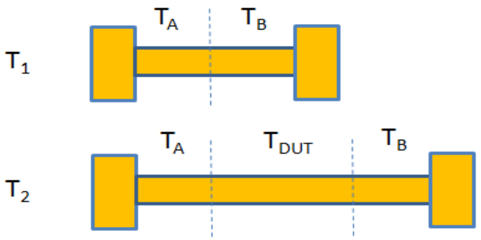


$$L_{DUT} = L_{LONG} - L_{SHORT}$$



Eigenvalue solution: not de-embedding
For calculating trace attenuation only

- Convert S to T for short and long trace structures
- Assume the left (and right) sides of short and long trace structures are identical
- Assume DUT is uniform transmission line
- Trace-only attenuation is written in one equation.



$$T_1 = T_A \cdot T_B$$
$$T_2 = T_A \cdot T_{DUT} \cdot T_B$$
$$\Rightarrow \quad T_2 \cdot T_1^{-1} = T_A \cdot T_{DUT} \cdot T_A^{-1}$$

For uniform transmission line:

$$T_{DUT} = P \cdot \begin{pmatrix} e^{-\gamma l} & 0 \\ 0 & e^{+\gamma l} \end{pmatrix} \cdot P^{-1}$$

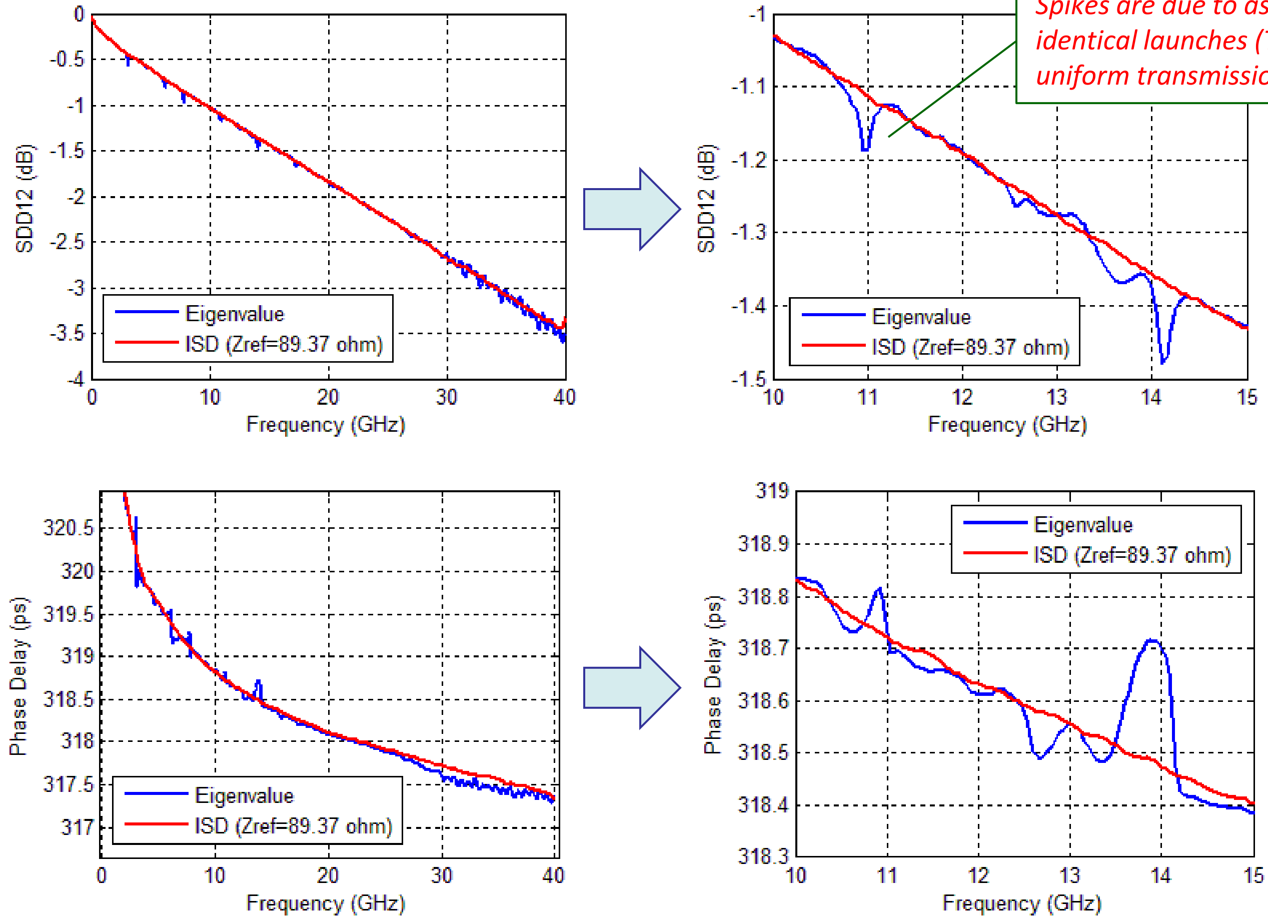
Let $T_2 \cdot T_1^{-1} = \begin{pmatrix} a & b \\ c & d \end{pmatrix}$

$$\Rightarrow \quad e^{-\gamma l} = \frac{(a+d) \pm \sqrt{(a-d)^2 + 4bc}}{2}$$

eigenvalue

modal propagation constant

Case 1: 2” (=7”-5”) trace attenuation
Eigenvalue solution is prone to spikes



Spikes are due to assumptions of identical launches (T_A and T_B) and uniform transmission line (T_{DUT}).

ISD’s spikes-free results help DK and DF extraction later.

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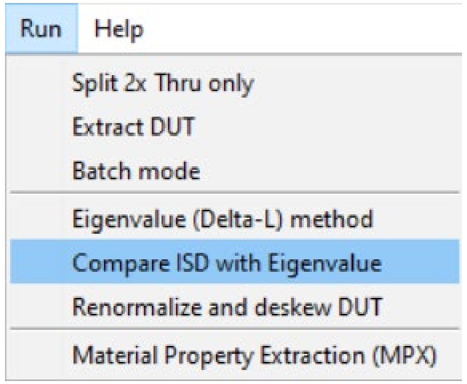
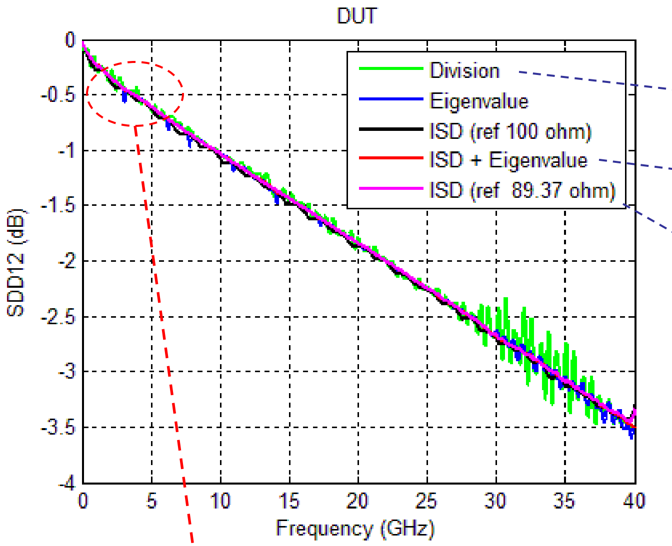
One click compares ISD with eigenvalue and more…



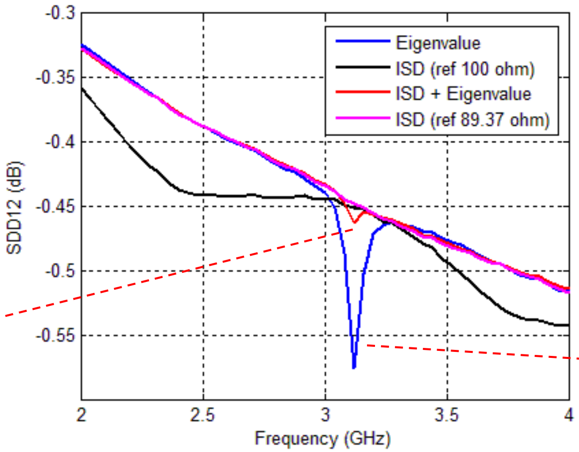
One click does it all



Direct dB subtraction

Eigenvalue of ISD results

Renormalize ISD results by trace impedance (automatically calculated)



Spikes are due to assumption of uniform transmission line (T_{DUT}).

Spikes are due to assumptions of identical launches (T_A and T_B) and uniform transmission line (T_{DUT}).

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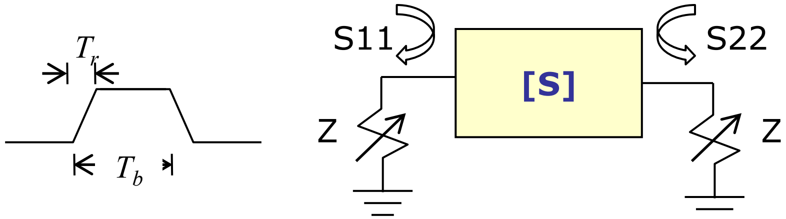
How to define trace impedance
PCB trace is non-uniform transmission line

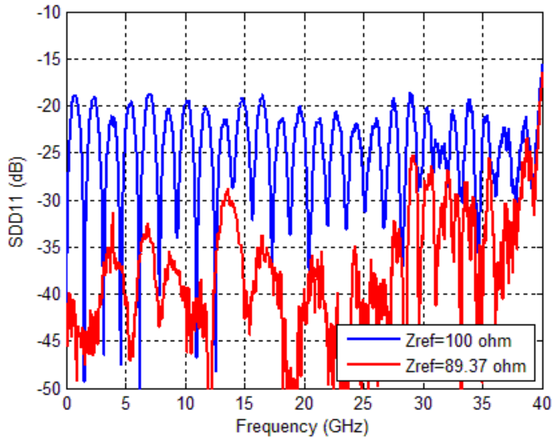
- Define impedance by minimal RL*

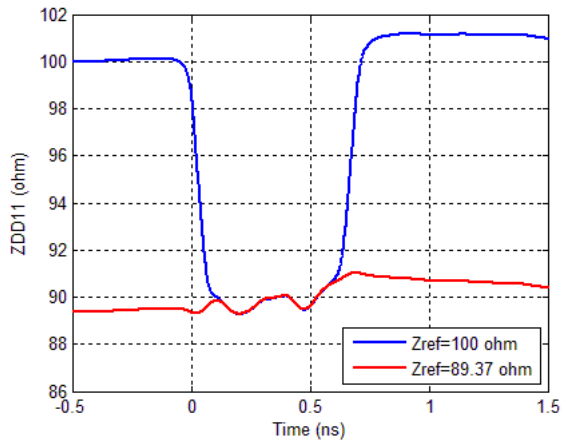


Minimize:

$$\varphi = \int_{f_{\min}}^{f_{\max}} \left\{ \left| S_{11}(f) \right|^2 + \left| S_{22}(f) \right|^2 \right\} \cdot \left| w(f) \right|^2 df$$

$$w(f) = \frac{\sin(\pi f T_r)}{\pi f T_r} \cdot \frac{\sin(\pi f T_b)}{\pi f T_b}$$

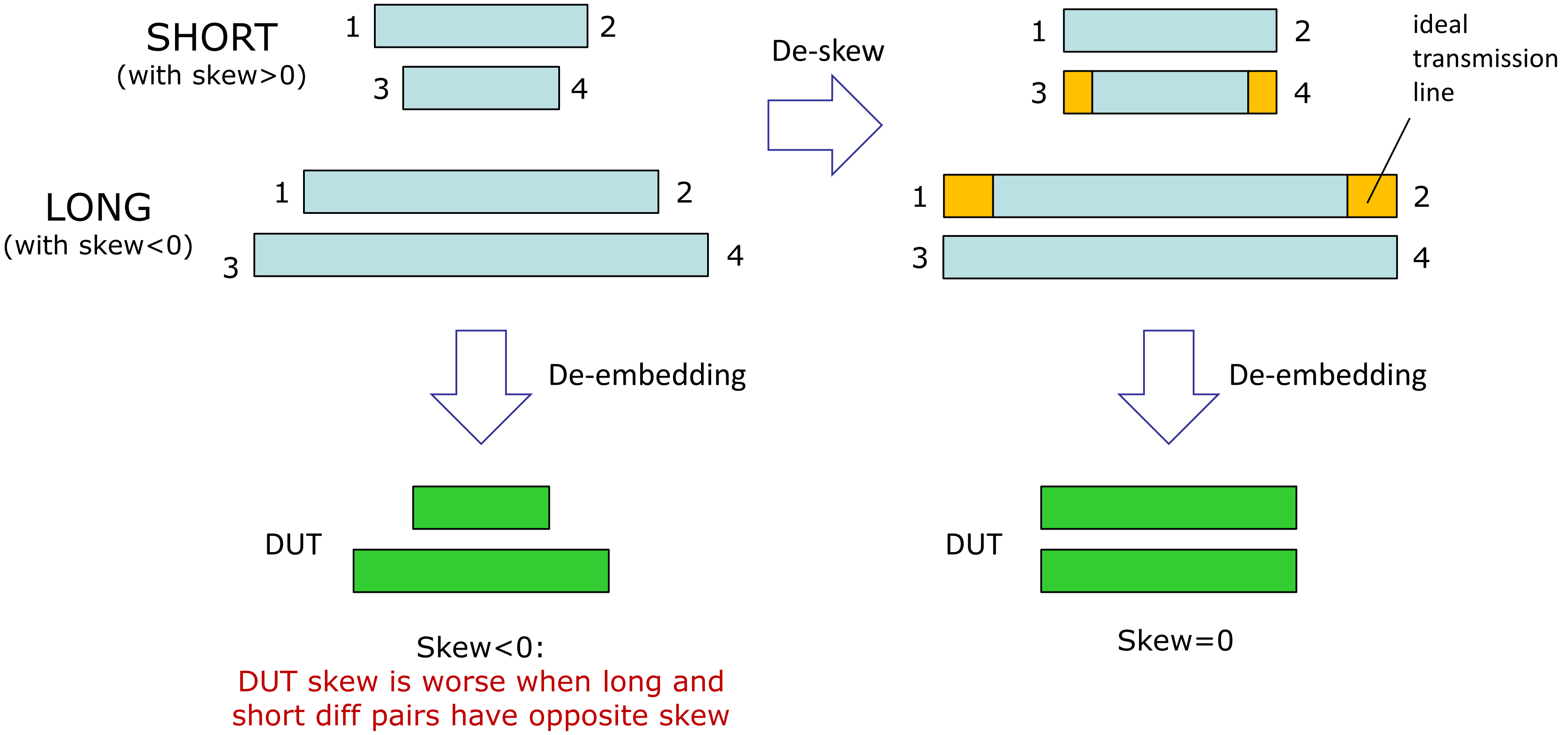




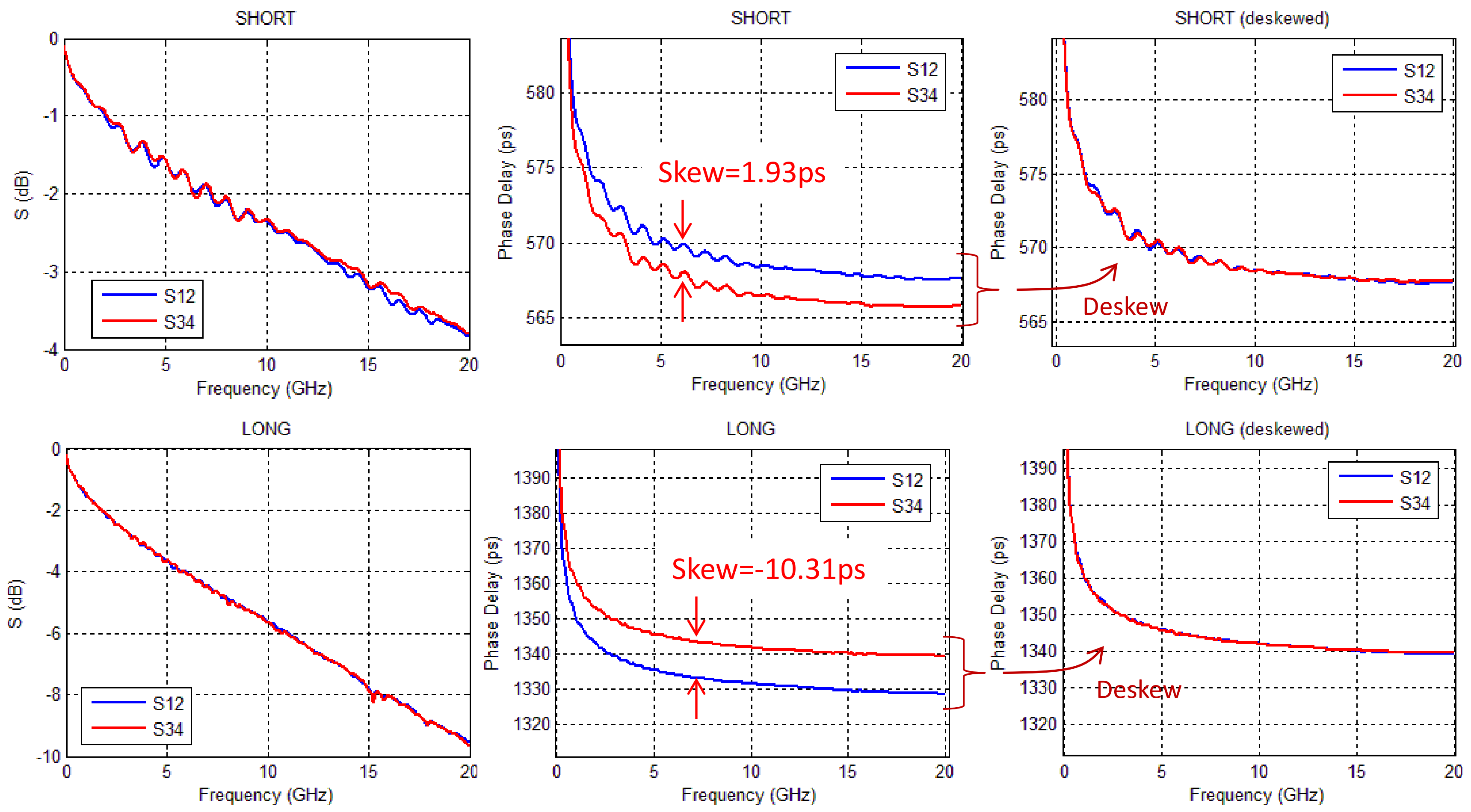
* J. Balachandran, K. Cai, Y. Sun, R. Shi, G. Zhang, C.C. Huang and B. Sen, “Aristotle: A fully automated SI platform for PCB material characterization,” DesignCon 2017, 01/31-02/02/2017, Santa Clara, CA.

Skewless de-embedding

- Pad ideal transmission line to de-skew.

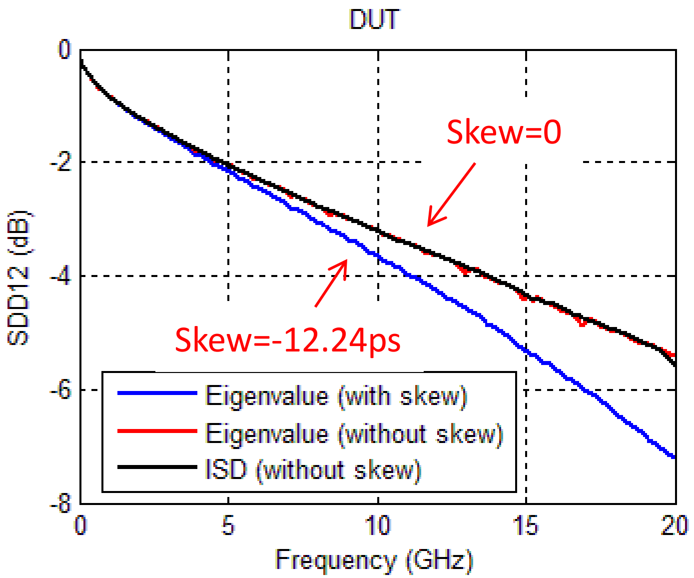


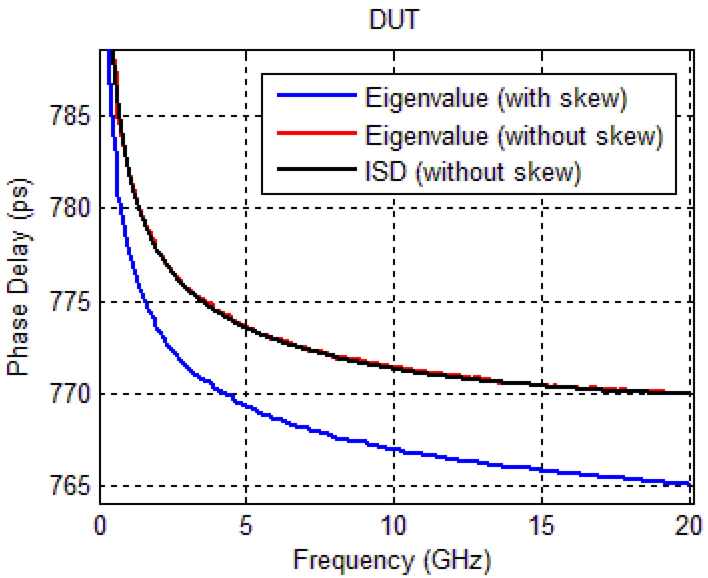
ISD optionally automates de-skewing of raw data

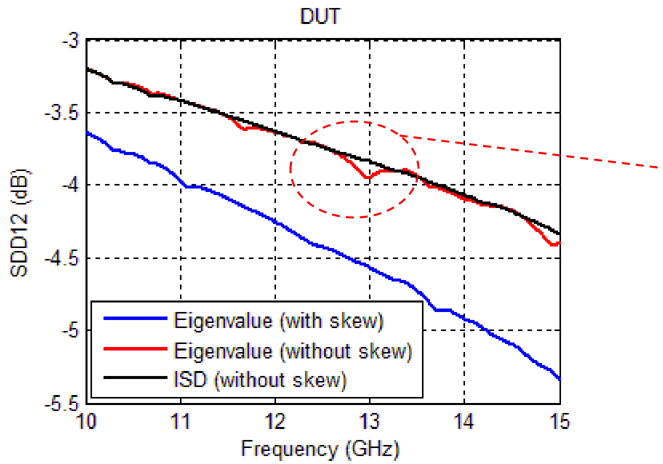


LONG=8”
SHORT=3”

Case 2: Extracted trace attenuation can be very different with or without skew

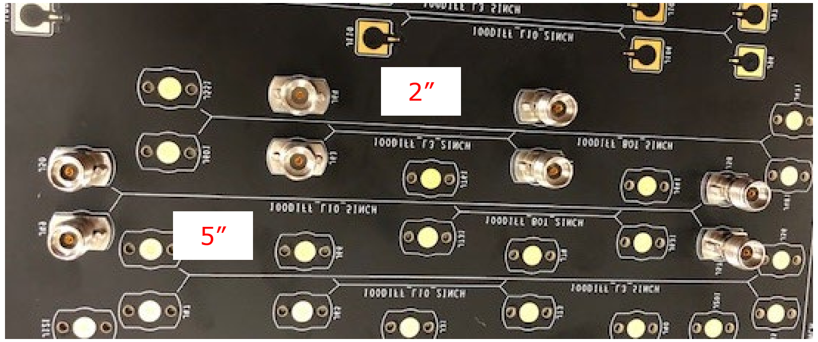


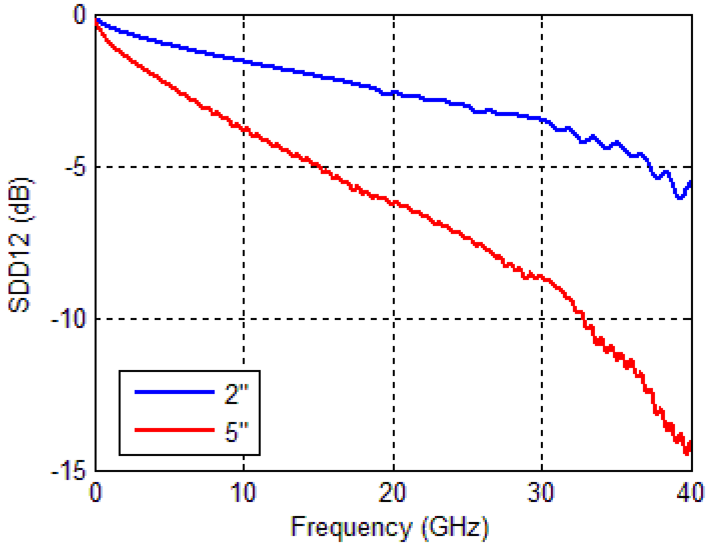


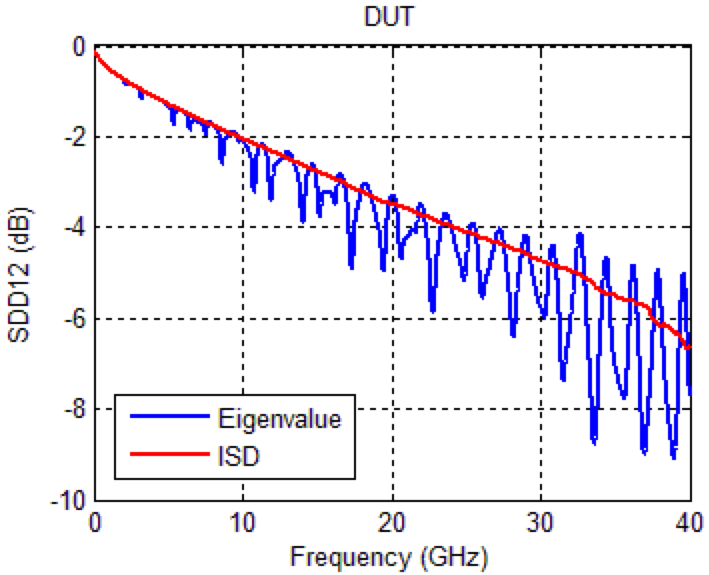


Eigenvalue solution has a dip at the frequency of interest (~12.9 GHz)

Case 3: Eigenvalue (Delta-L) solution becomes unstable in this case, but why?

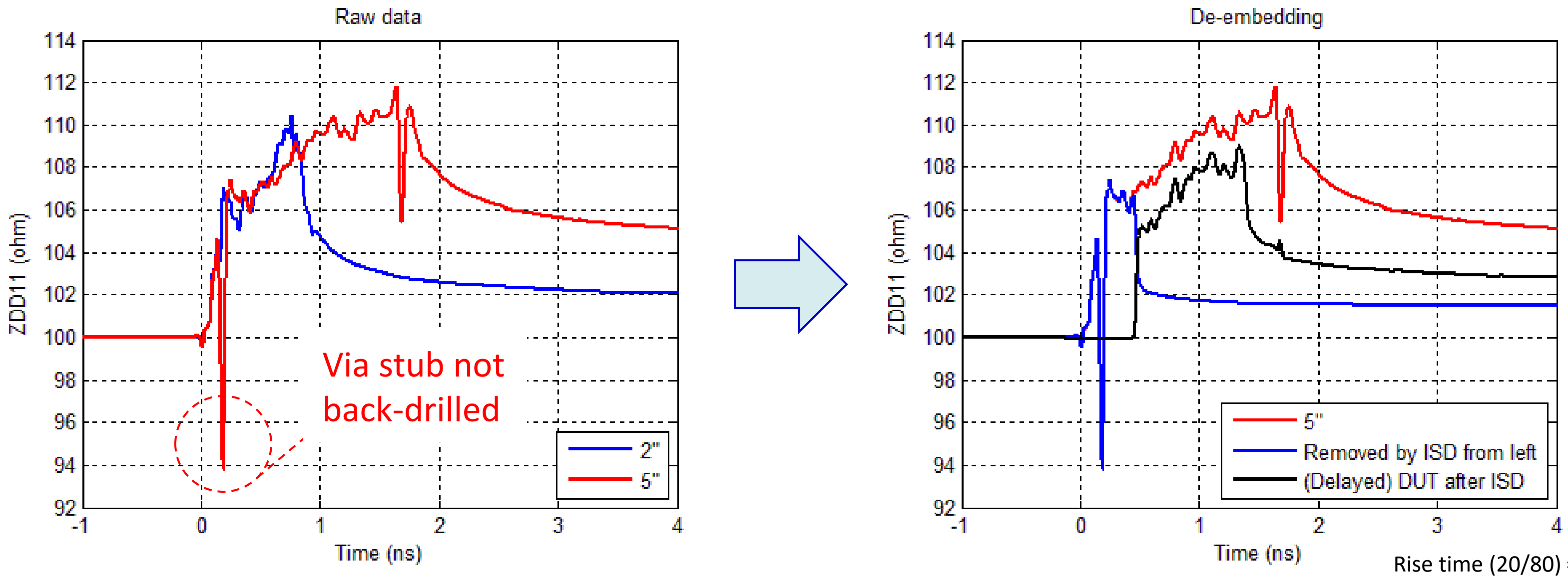






TDR of raw data reveals why…
2″ structure was back-drilled but 5″ was not

- Eigenvalue solution assumes 2″ and 5″ structures have identical launches.
- ISD de-embeds 5″ structure's launch correctly.

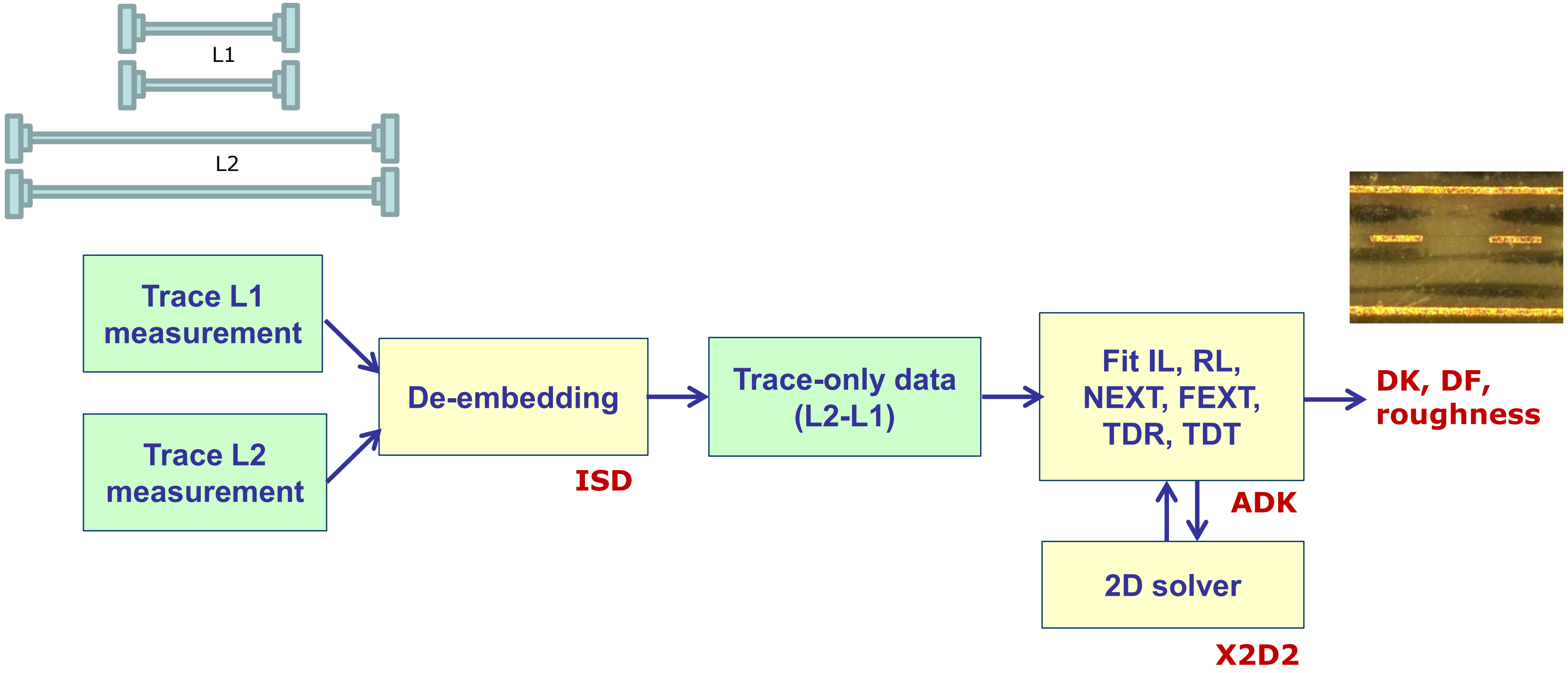


Rise time (20/80) = 20 ps

ISD saves $$$ and time for not spinning another board.

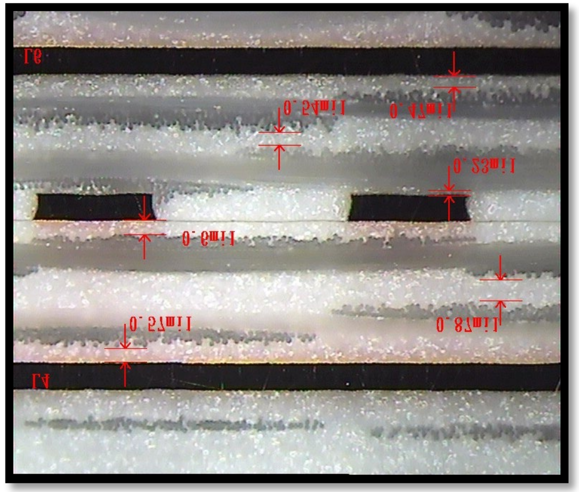
Example 7: Material property extraction
DK, DF and roughness

- Self consistent approach to extract DK, DF and roughness by matching all IL, RL, NEXT, FEXT and TDR/TDT of de-embedded trace-only data.

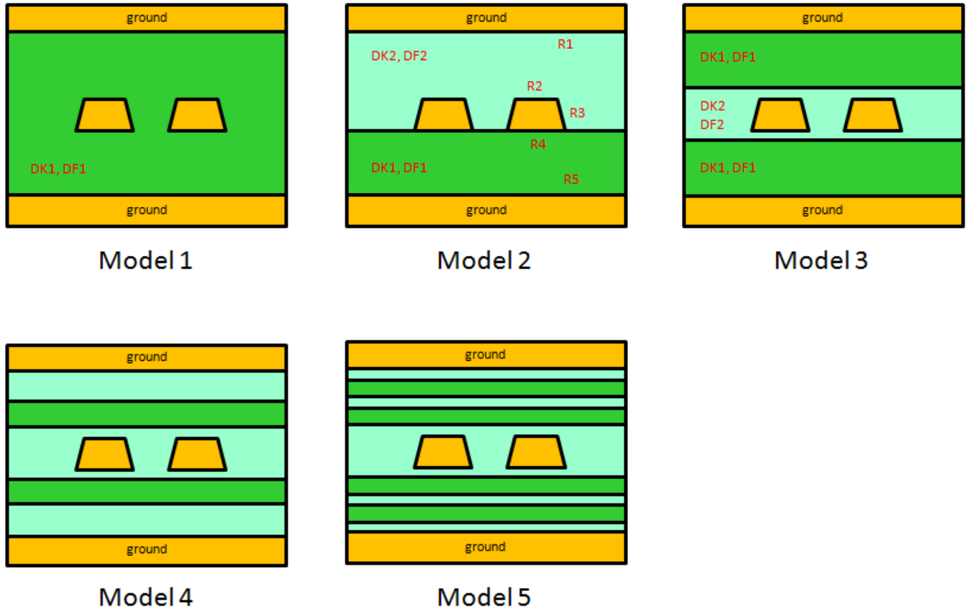


Automated extraction flow

Models for cross section



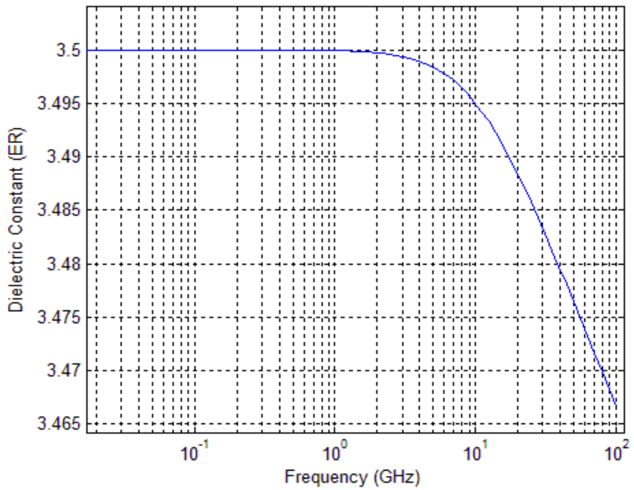
Optimized variables:
DK1, DF1, DK2, DF2
R1, R2, R3, R4, R5 (roughness)
Metal width and spacing

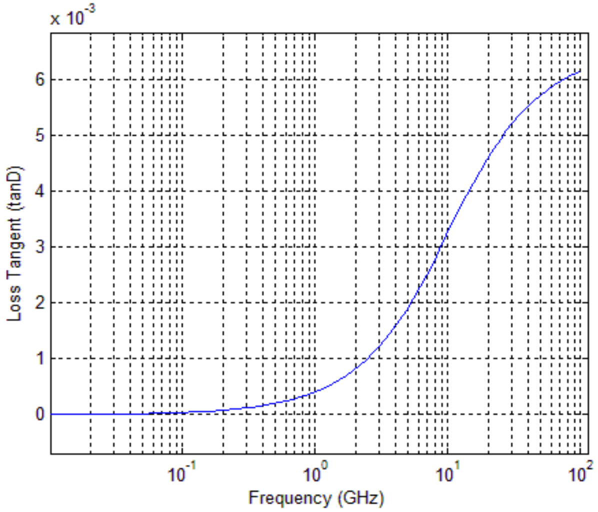


Causal dielectric model

- Wideband Debye (or Djordjevic-Sarkar) model
  - Need only four variables: ε_∞ , $\Delta\varepsilon$, m_1 , m_2

$$\varepsilon = \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f}\right)$$
$$= \varepsilon_r \cdot \left(1 - i \cdot \tan\delta\right)$$





$$\varepsilon_\infty = 3.35 \ , \ \Delta\varepsilon = 0.15 \ , \ m_1 = 10 \ , \ m_2 = 14.5$$

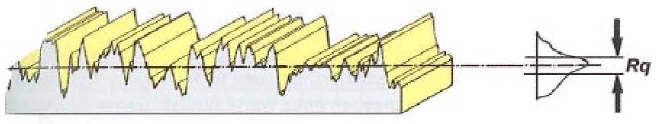
Surface roughness model

- Effective conductivity (by G. Gold & K. Helmreich at DesignCon 2014) needs only two variables: σ_{bulk} , R_q

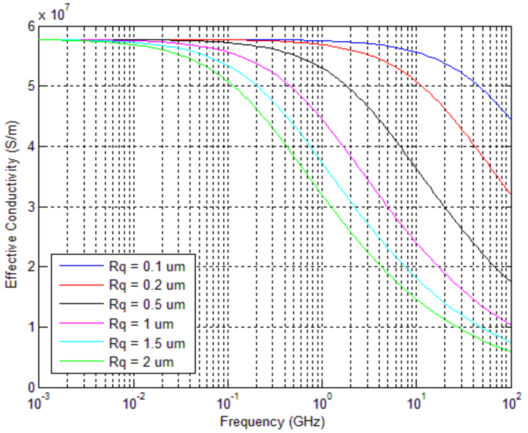
Parameter	Description	Standard
R_q	root mean square	DIN EN ISO 4287
R_a	arithmetic average	DIN EN ISO 4287, ANSI B 46.1
R_k	core roughness depth	DIN EN ISO 13565
R_z	average surface roughness	DIN EN ISO 4287

Table 1: *Statistical parameters to describe surface roughness*

$$\sigma(x)=\sigma_{bulk}\cdot CDF(x)=\sigma_{bulk}\cdot\int_{-\infty}^{x} PDF(x)du=\sigma_{bulk}\cdot\int_{-\infty}^{x} e^{-\frac{u^2}{2R_q^2}}du$$



- Numerically solving $\nabla^2\overline{B}-j\omega\mu\sigma\overline{B}+\frac{\nabla\sigma}{\sigma}\times\left(\nabla\times\overline{B}\right)=0$ and equating power to that of smooth surface gives σ_{eff}



$\sigma_{bulk}=5.8\times10^{7}$ s/m

- ❖ Simple
- ❖ Work well with field solver
- ❖ Give effect of roughness on all IL, RL, NEXT and FEXT

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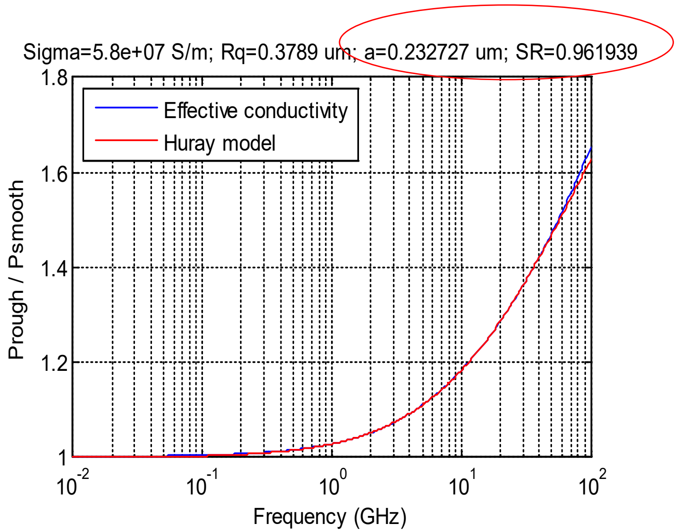
Convert effective conductivity to Huray model

- Huray model

$$\frac{P_{rough}}{P_{smooth}} \approx 1 + \frac{3}{2} \cdot SR \cdot \left(\frac{1}{1 + \frac{\delta(f)}{a} + \frac{1}{2}\left(\frac{\delta(f)}{a}\right)^2} \right)$$

$$\delta(f) = \sqrt{\frac{1}{\pi f \mu \sigma}} \quad ; \quad a = \text{radius} \quad ; \quad SR = \text{surface ratio}$$

- Curvefit* Prough / Psmooth to convert σ_{bulk} , R_q to a , SR



*Automated in ADK

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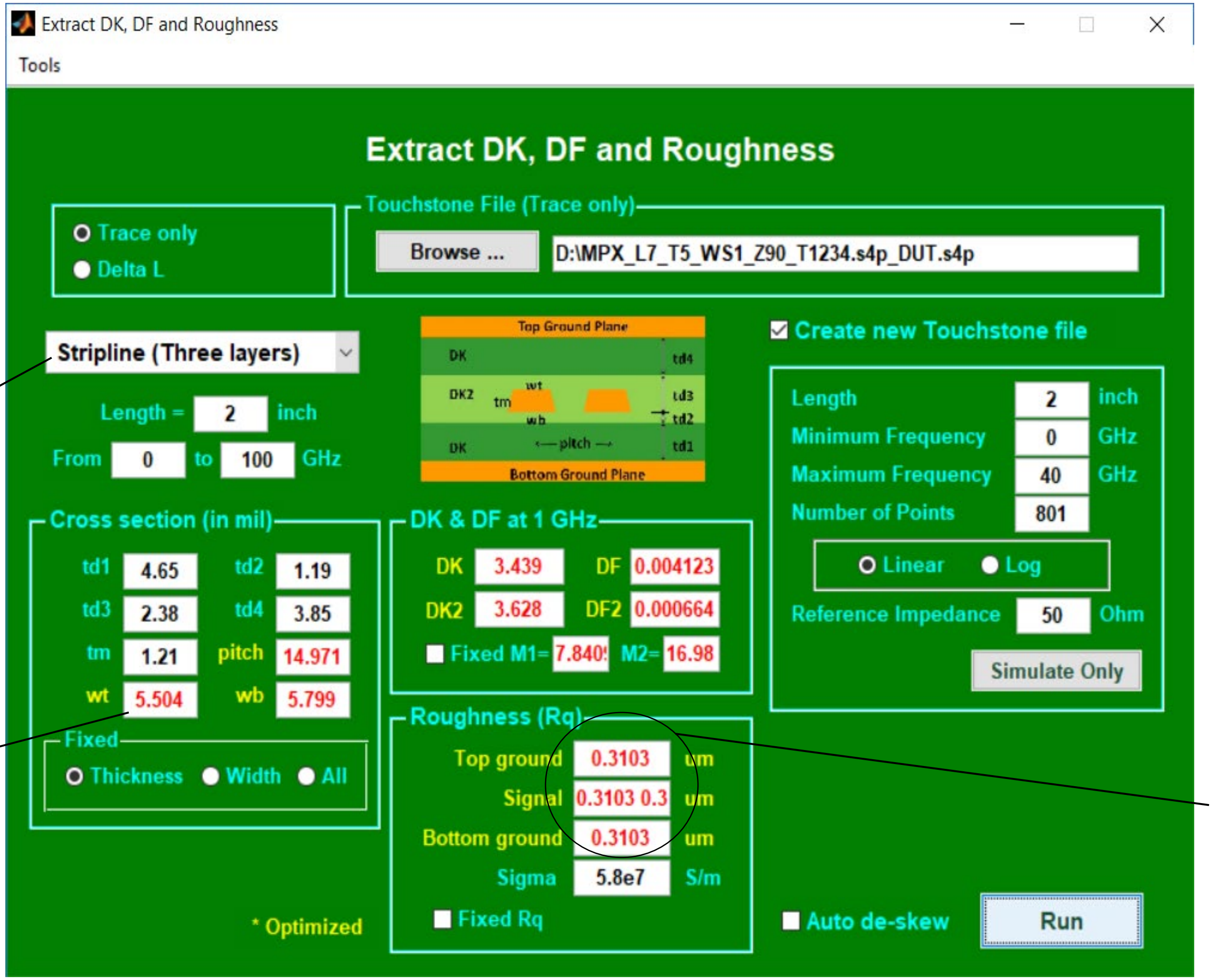
DK/DF/SR extraction (from ADK)

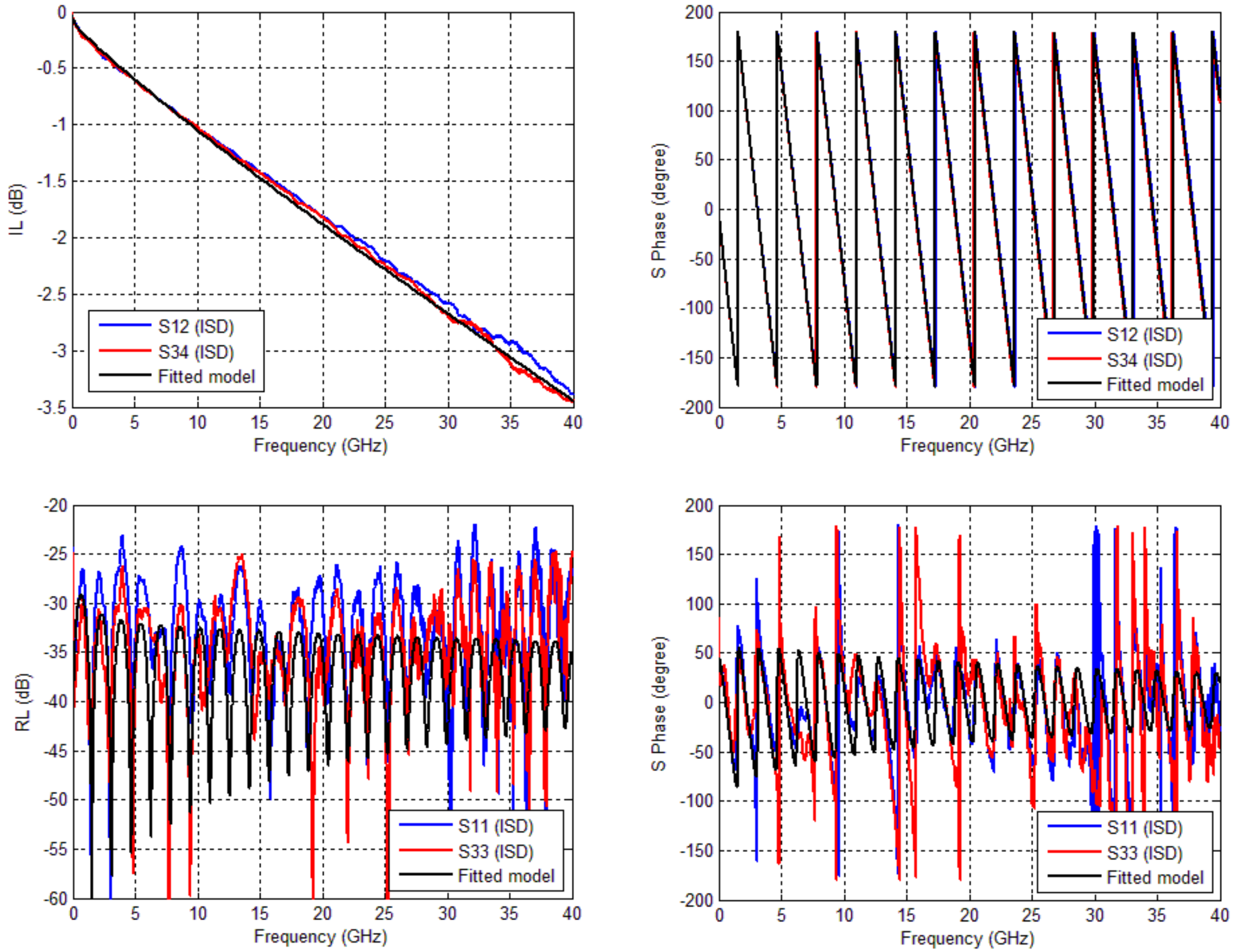


Multiple templates

Updated after extraction

Different roughness for each surface

Matching IL and RL



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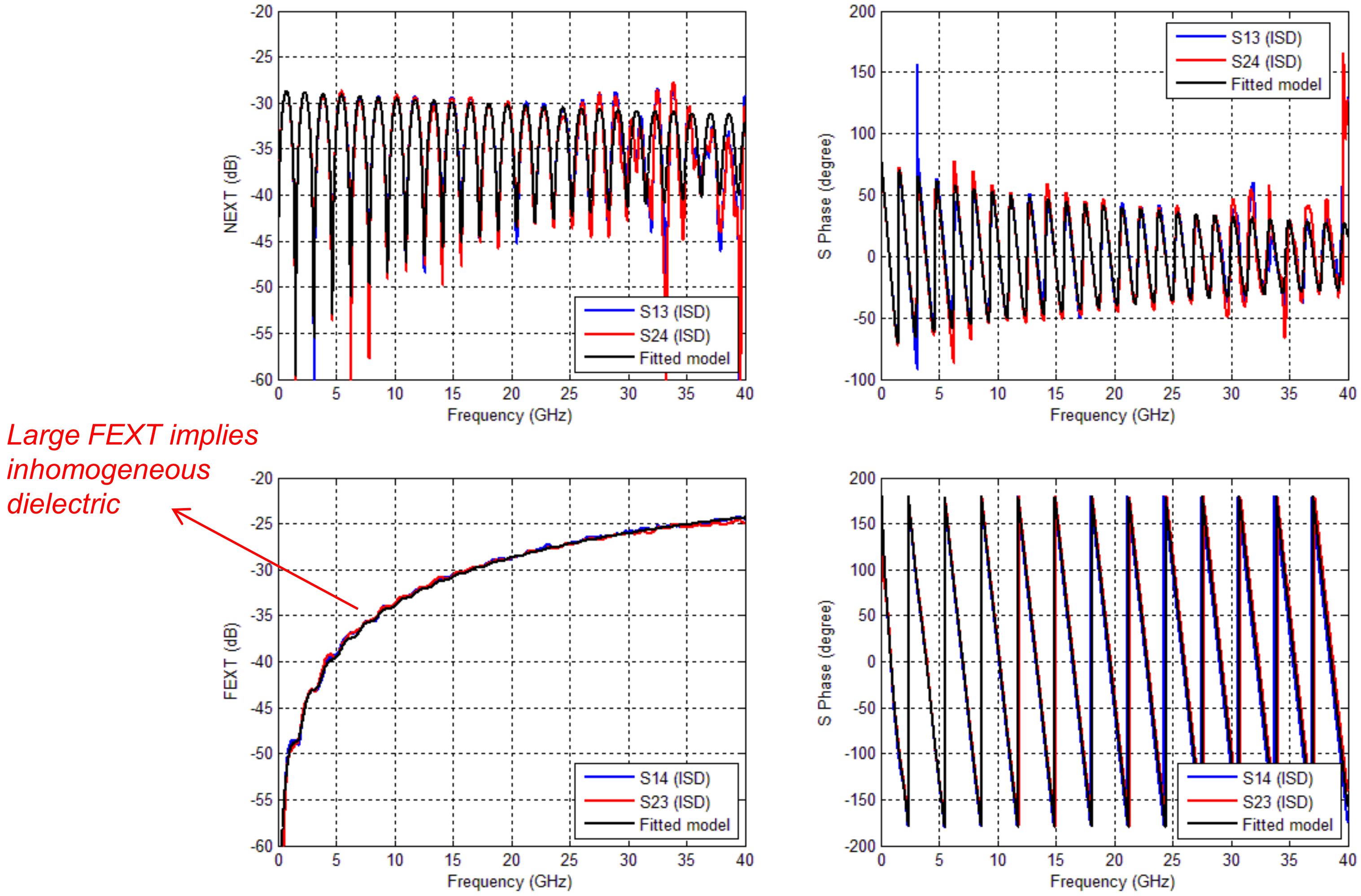
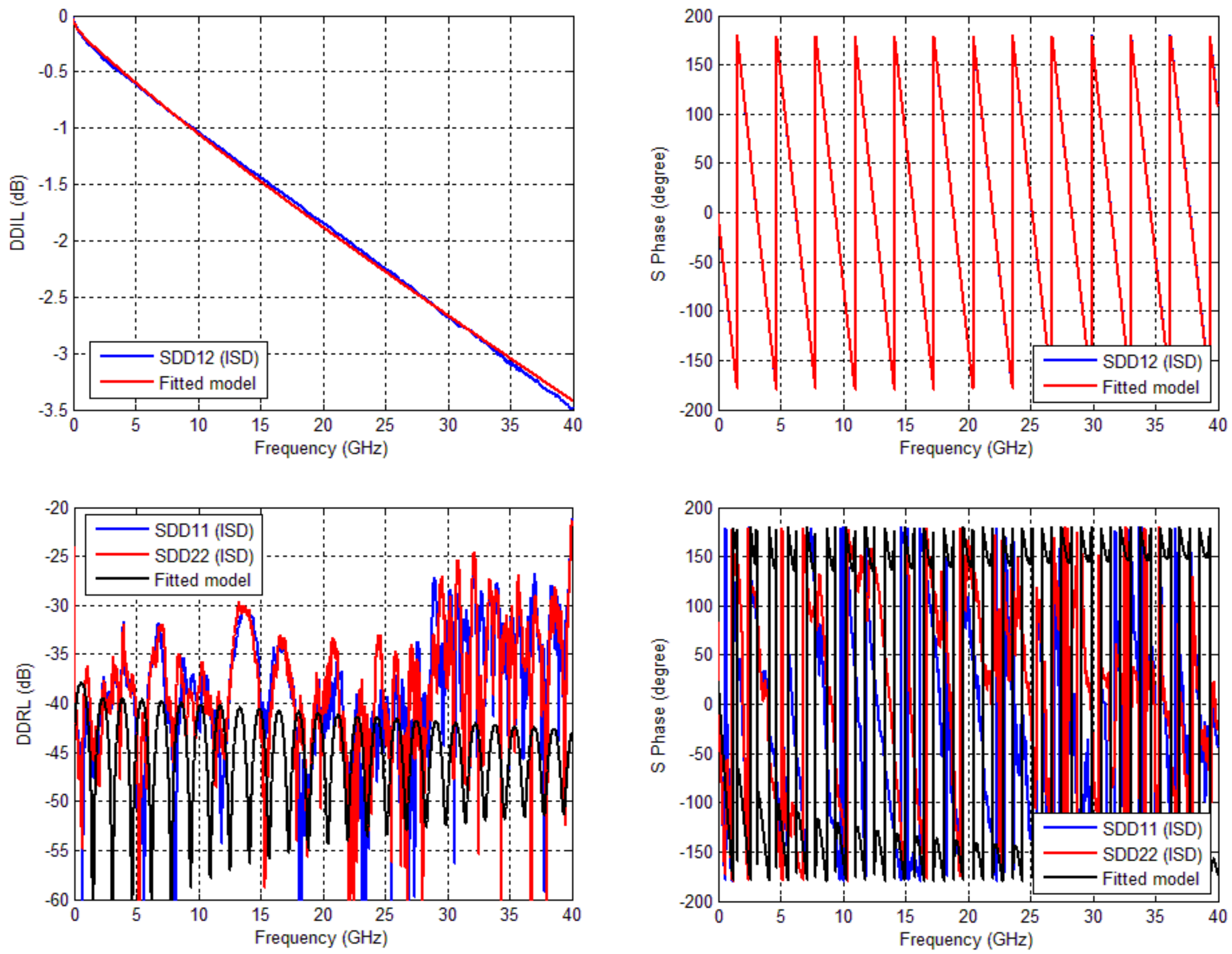
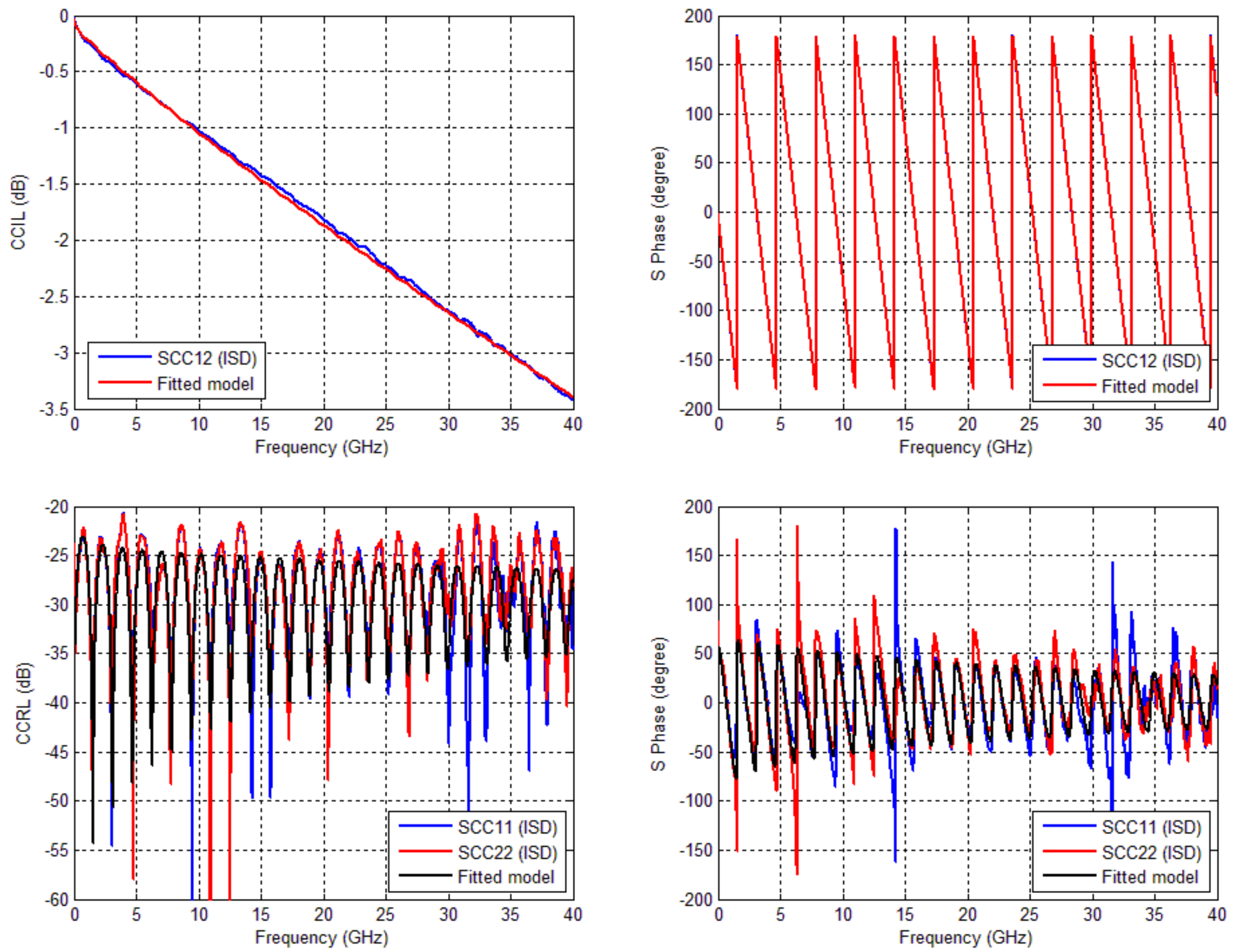
Matching NEXT and FEXT



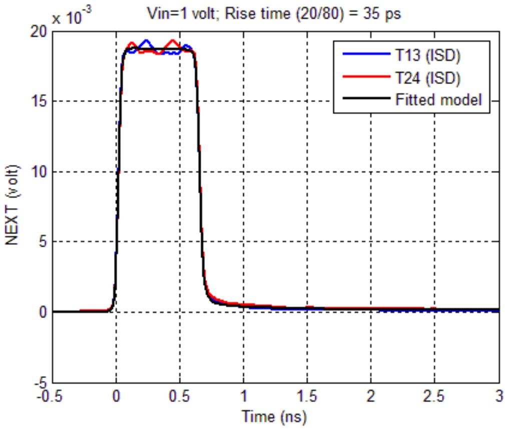
Matching DDIL and DDRL

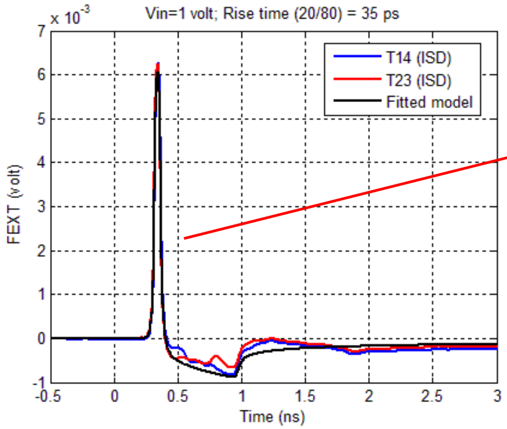


Matching CCIL and CCRL

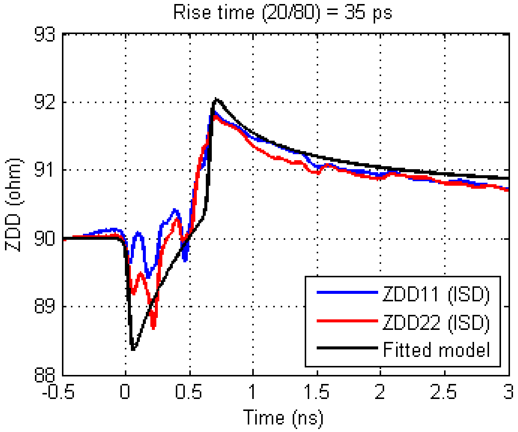


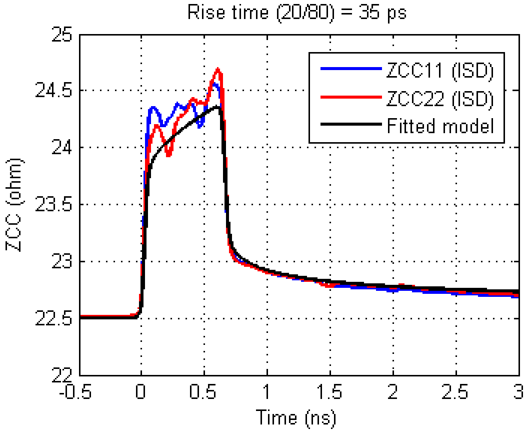
Matching TDT and TDR

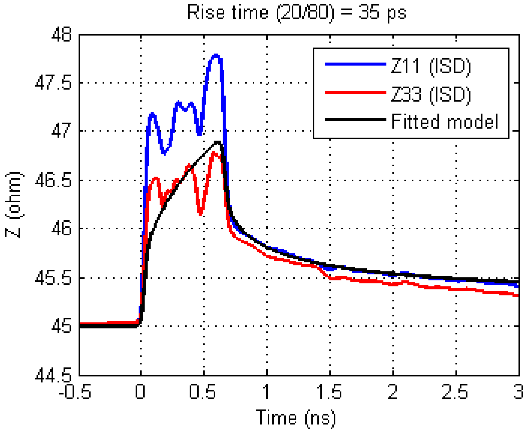




Positive polarity implies $K_C > K_L$

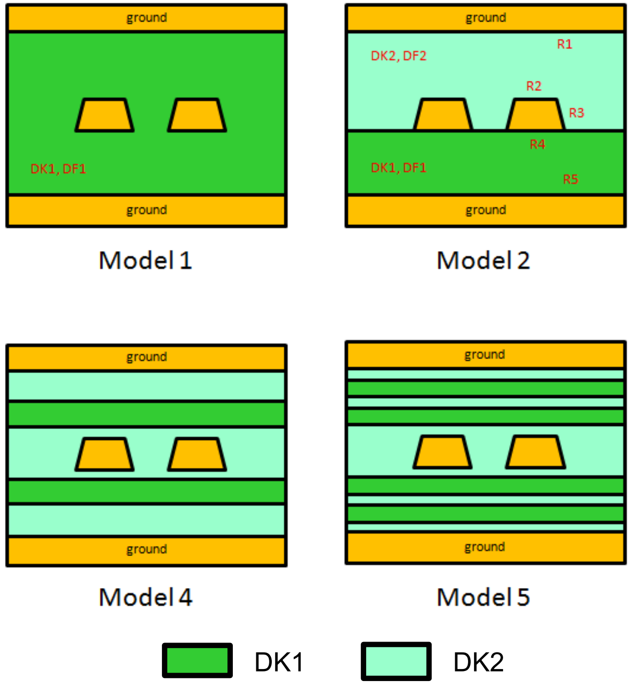


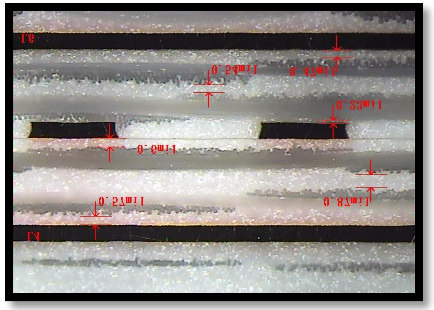




Comparison of Models 1 to 5

- Model 1 cannot match FEXT. Models 2 to 5 can match all IL, RL, NEXT, FEXT and TDR/TDT very well.



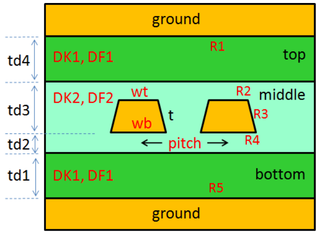


Model	DK1	DK2
1	3.510	-
2	2.444	4.294
3	3.413	3.623
4	3.863	3.360
5	3.115	3.975

At 10 GHz

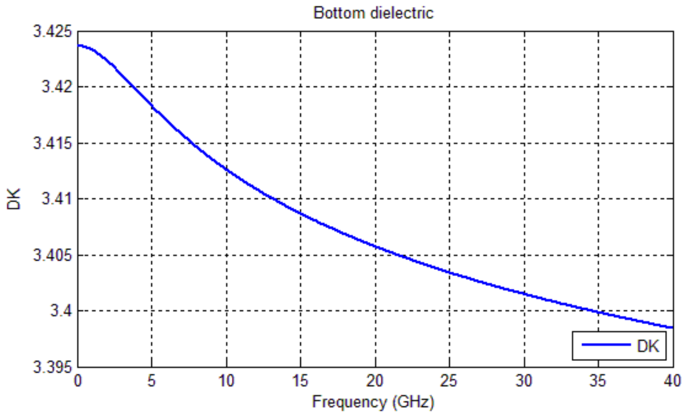
DK2>DK1 because of positive-polarity FEXT

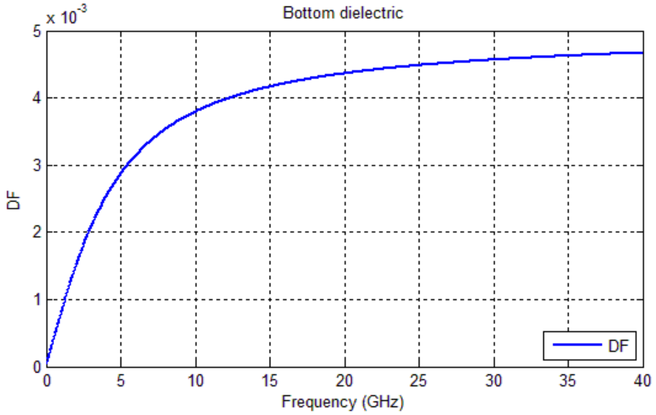
Extracted DK1 and DF1
Model 3



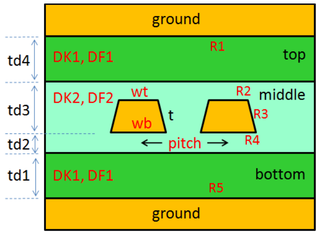
$$\varepsilon_\infty = 3.27929$$
$$\Delta\varepsilon = 0.144348$$
$$m1 = 9.58619$$
$$m2 = 15.4109$$

$$\varepsilon = \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f}\right)$$
$$= \varepsilon_r \cdot (1 - i \cdot \tan\delta)$$



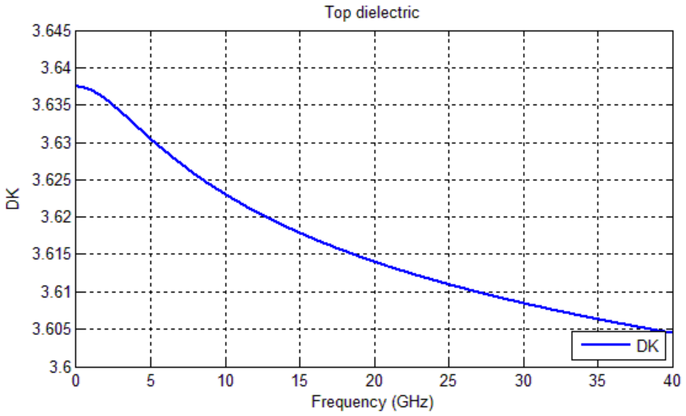


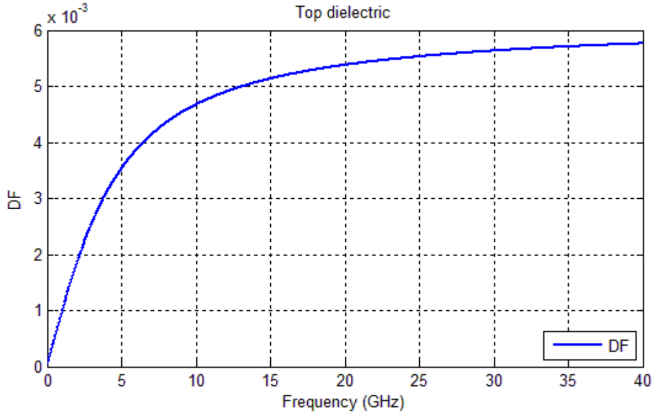
Extracted DK2 and DF2
Model 3



$$\varepsilon_\infty = 3.46724$$
$$\Delta\varepsilon = 0.170196$$
$$m1 = 9.58715$$
$$m2 = 14.8352$$

$$\varepsilon = \varepsilon_\infty + \Delta\varepsilon \cdot \frac{1}{m_2 - m_1} \cdot \log_{10}\left(\frac{10^{m_2} + i \cdot f}{10^{m_1} + i \cdot f}\right) = \varepsilon_r \cdot (1 - i \cdot \tan\delta)$$





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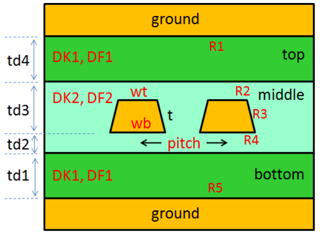
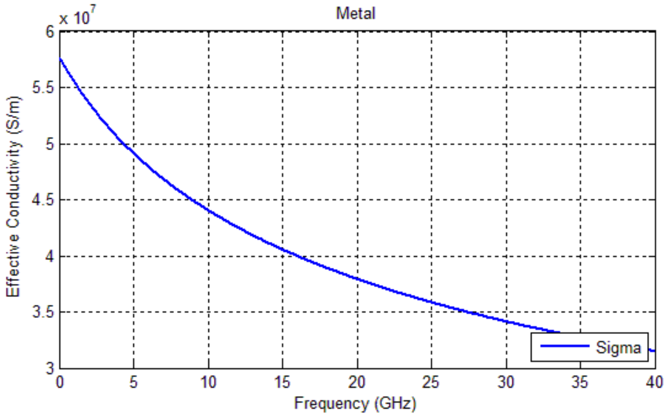
Extracted effective conductivity
Model 3

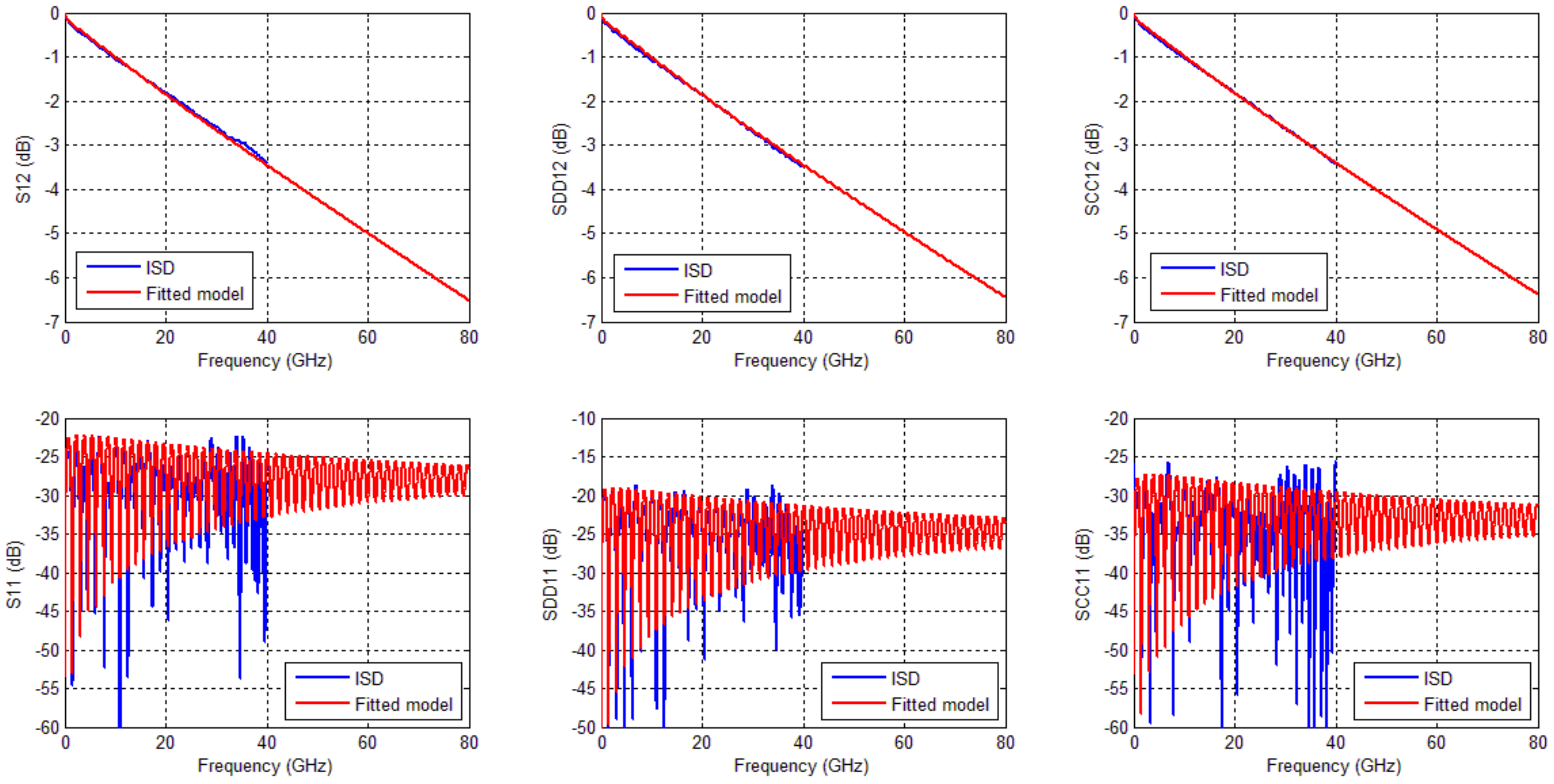


$$\sigma = 5.8 \times 10^7 \text{ S/m}$$

$$R_q = 0.324321\, \mu\text{m}$$



Length- and frequency-scalable models can now be created.



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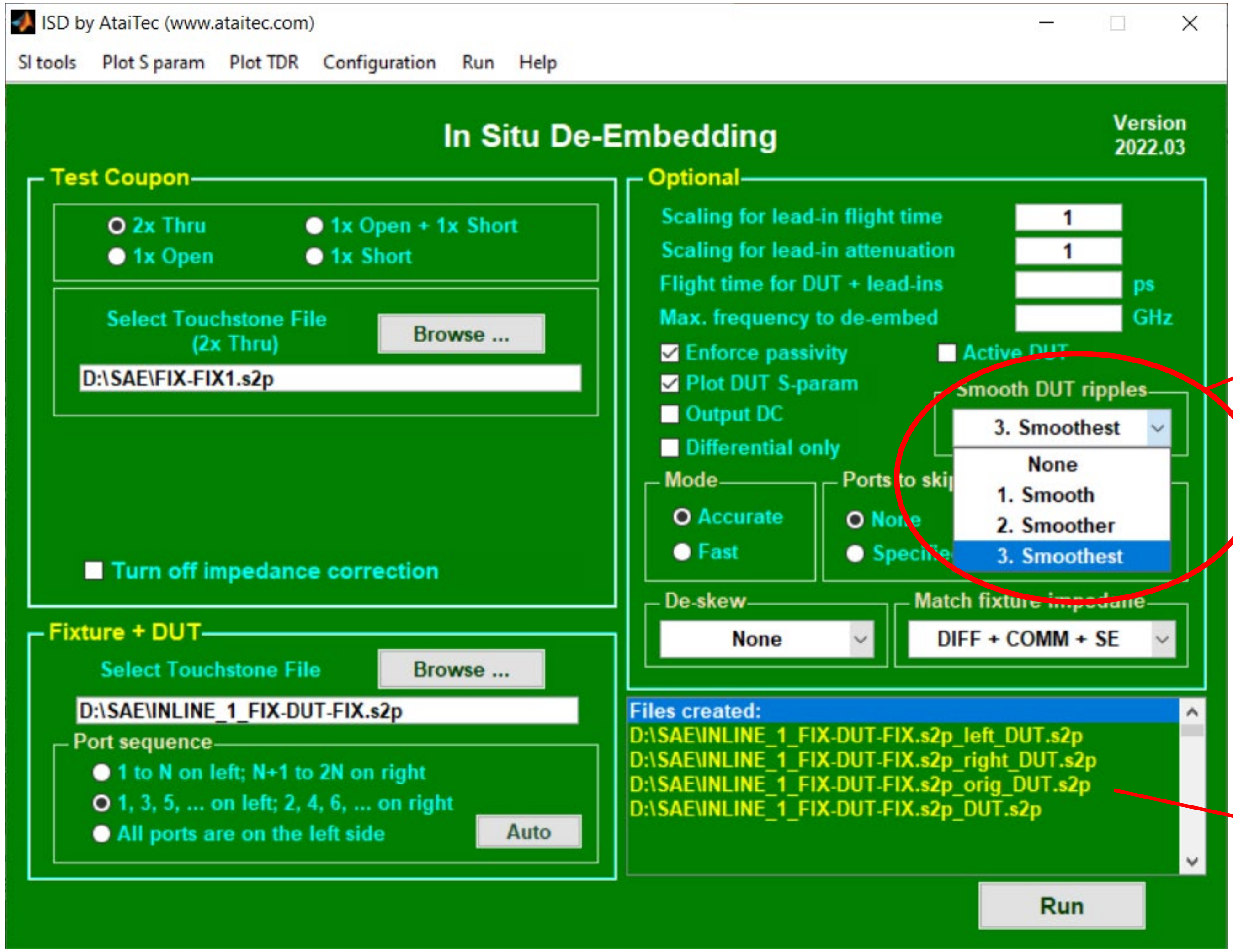
New “Smoothing” feature improves accuracy for both raw measurement and de-embedded data

- S parameters can have artificial ripples
  - Before de-embedding
    - Due to bad calibration, port extension, bad contact or cable movement
  - After de-embedding
    - Due to 2x thru’s IL and RL crossing each other or DUT much smaller than fixture
- New “Smoothing” feature lets the user remove such artificial ripples and improve data quality for both raw measurement and de-embedded DUT data.
- Better correlation, compliance testing and measurement-based simulation can now be achieved as a result.

"Smoothing" option

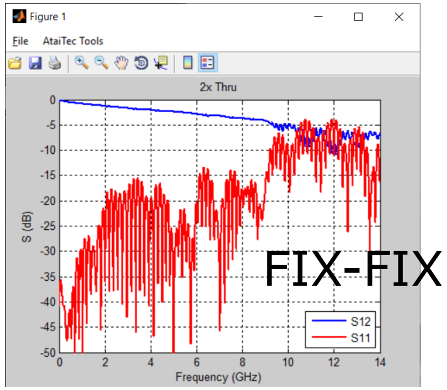


The user can choose different smoothing level for DUT.

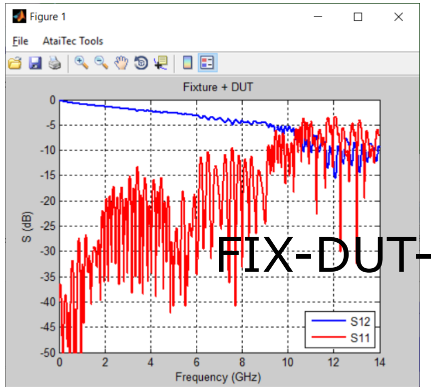
The original DUT file is saved in …_orig_DUT…

SAE/USCAR-49 inline connector example

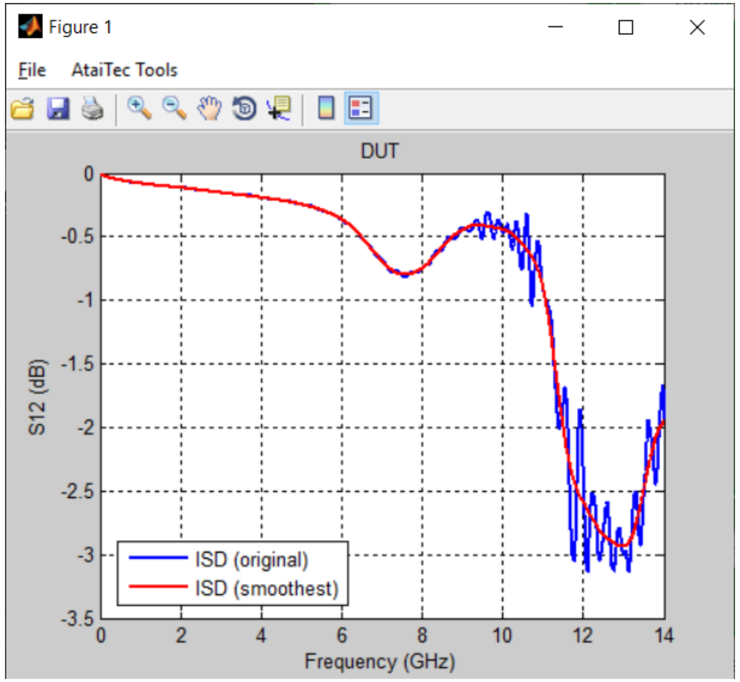
- ISD gives smooth IL and RL across all frequencies.

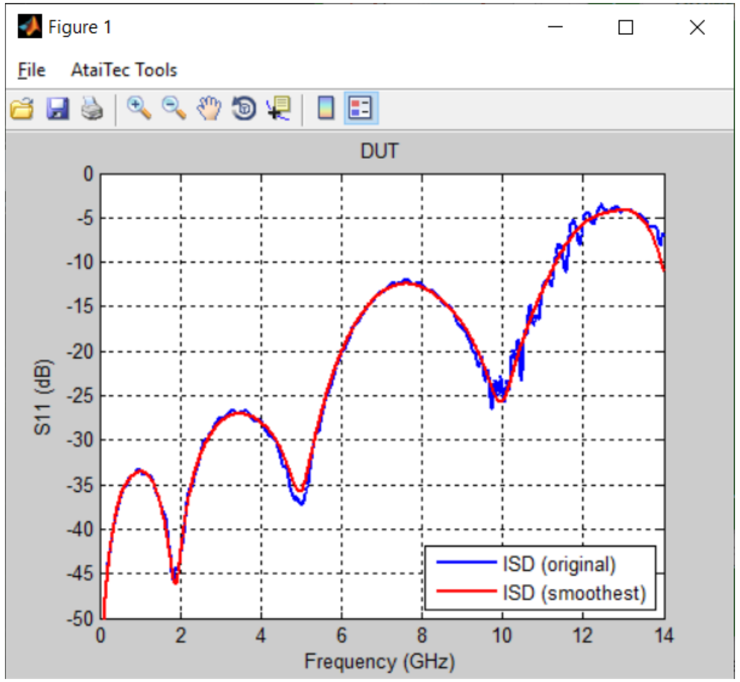


FIX-FIX



FIX-DUT-FIX





De-embedded DUT

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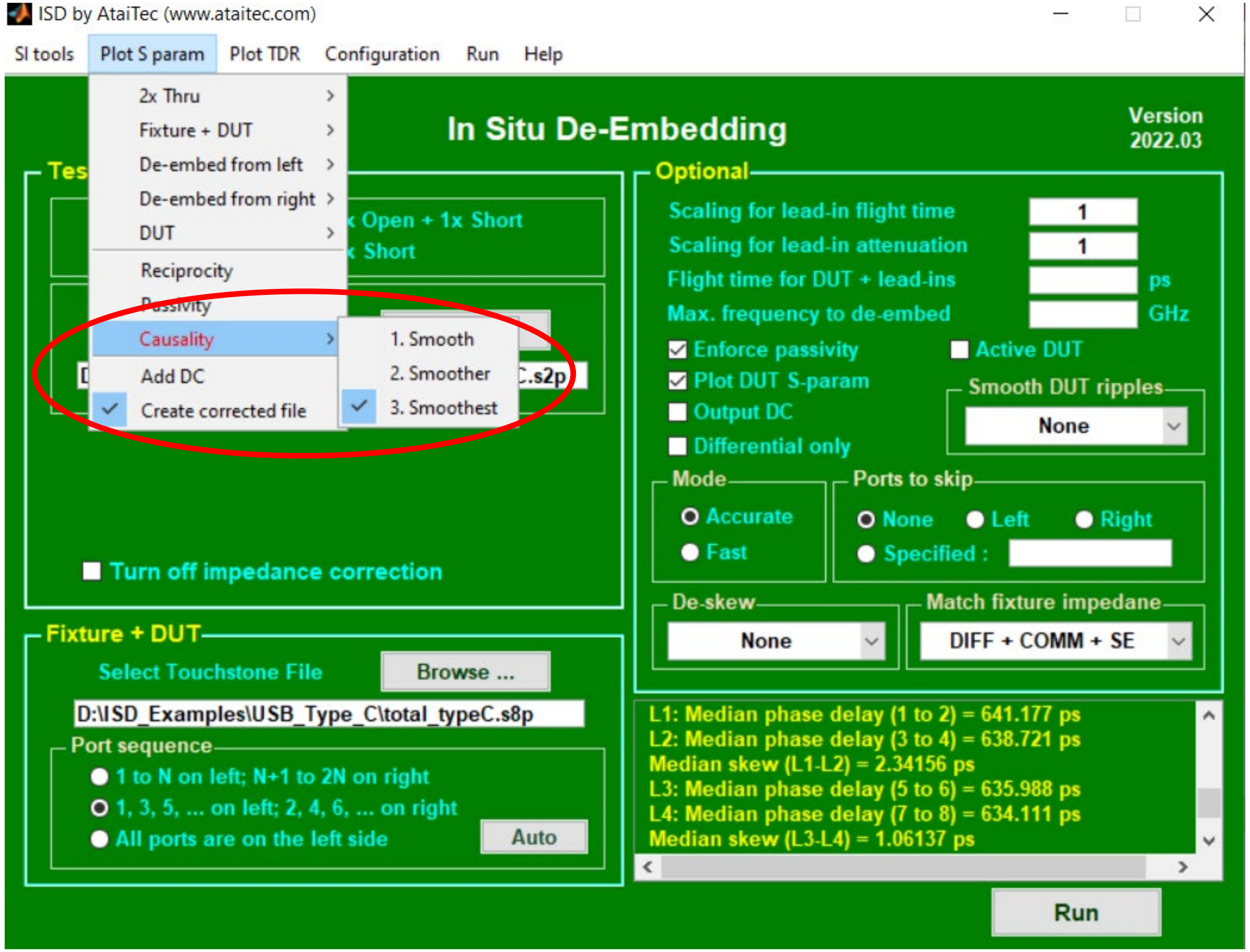
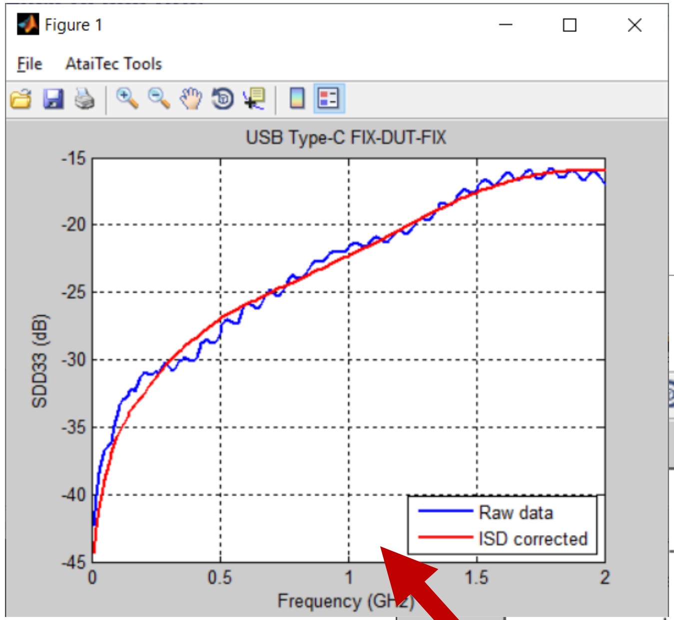
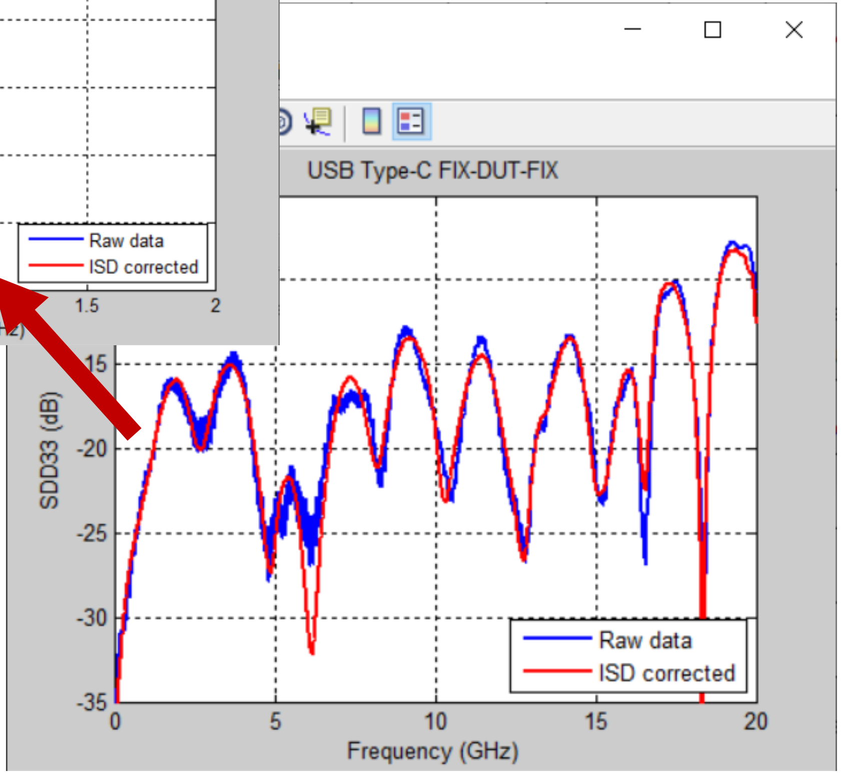
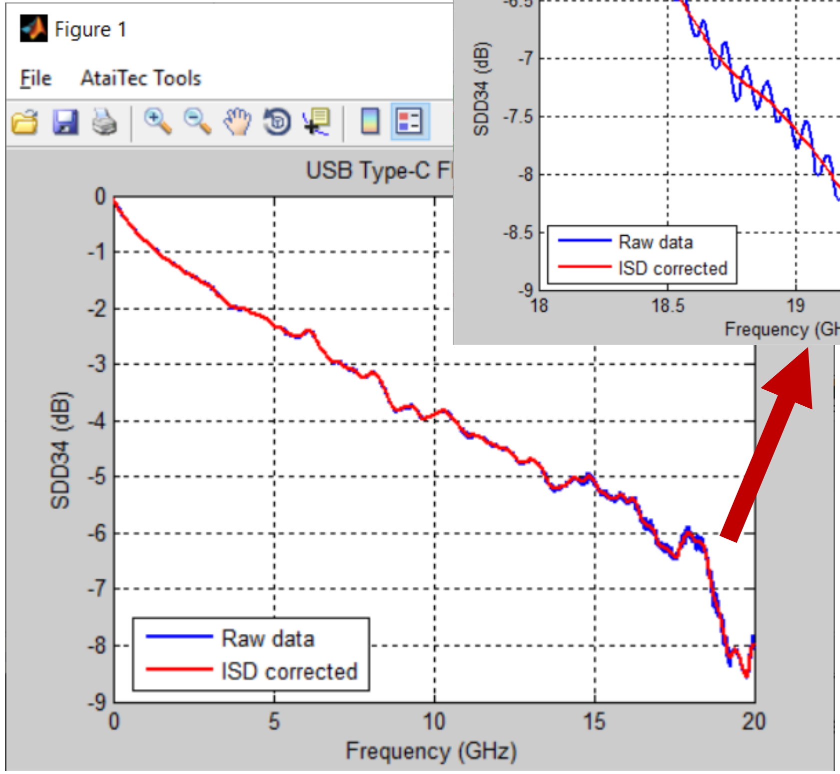
Both raw measurement and de-embedded DUT data can also be corrected through "Plot S param->Causality…"

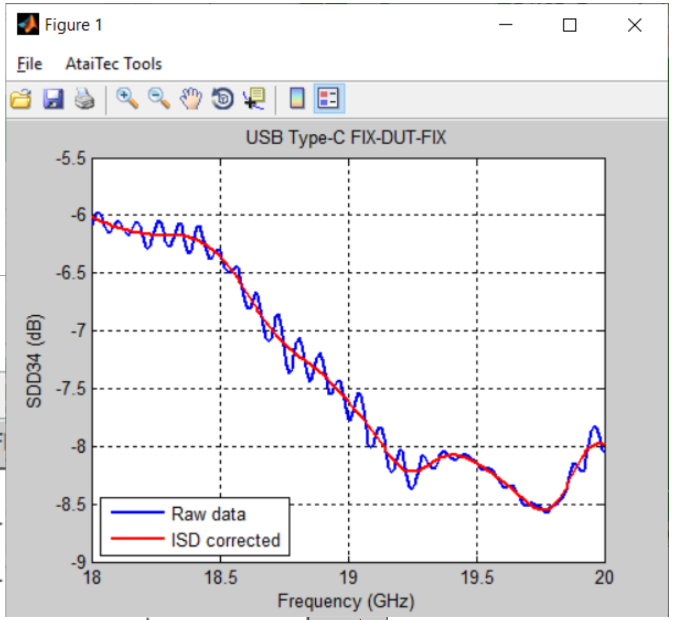


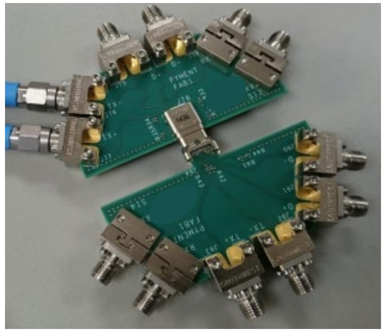
ISD corrects USB-C raw measurement in this example











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PCIe CEM 5.0 spec. requires de-embedded results

6.3.6. Signal Integrity Requirements and Test Procedures for 32.0 GT/s Support

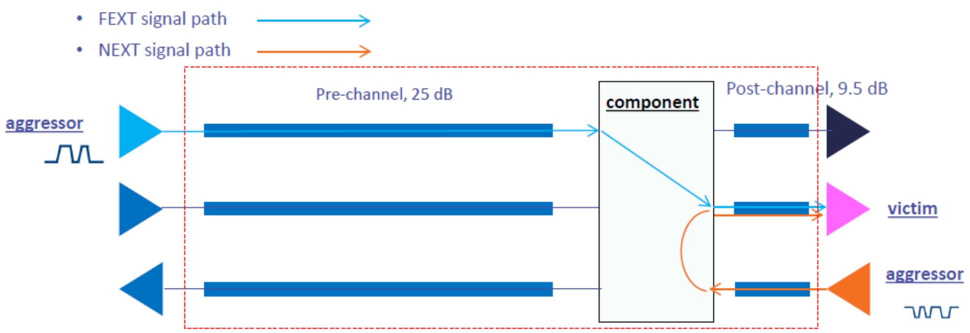
An electrical test fixture must be used for evaluating connector signal integrity. The test fixture effects are de-embedded from measurements. Test fixture requirements and recommendations are provided. Table 6-7 lists the electrical signal integrity parameters, requirements, and test procedures.

Table 6-7: Signal Integrity Requirements and Test Procedures for 32.0 GT/s Support

Parameter	Procedure	Requirements
Differential Insertion Loss (DDIL)	EIA 364-101 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement defined in Section 6.3.5.1. 3. The test fixture effect shall be removed from the measured S parameters. See Note 1.	[-0.1 - 0.05625 *f] dB up to 16 GHz; [3 – 0.25*f] dB for 16 < f < 24 GHz
Differential Return Loss (DDRL)	EIA 364-108 The EIA standard shall be used with the following considerations: 1. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. 2. The test fixture shall meet the test fixture requirement in Section 6.3.5.1. 3. The test fixture effect shall be removed. See Note 1.	[-20 + 0.625*f] dB up to 16 GHz; [-24 + 0.875*f] dB for 16 < f < 24 GHz
Intra-pair Skew	Intra-pair skew must be achieved by design; measurement not required.	5 ps max
Differential Near End Crosstalk (DDNEXT)	EIA 364-90 The EIA standard must be used with the following considerations: 1. The near end crosstalk requirement is with respect to all the adjacent differential pairs including the crosstalk from opposite sides of the connector, as listed in Table 6-6. 2. This is a differential crosstalk requirement between a victim differential signal pair and all its adjacent differential signal pairs. The measured differential S parameter shall be referenced to an 85 Ω differential impedance. 3. If this requirement is not met, $ccICN_{next}$ can be used to determine the crosstalk energy in the given frequency band using Equation 1.	[1.5*f – 60] dB up to 10 GHz; [(5/6)*f – 53.33] dB for 10 < f < 24 GHz; ccICNnext for fmax = 24 GHz < 250 µV

ISD accurately extracts pair-to-pair NEXT and FEXT for ccICN compliance testing

- ccICN: Component Contribution Integrated Crosstalk Noise



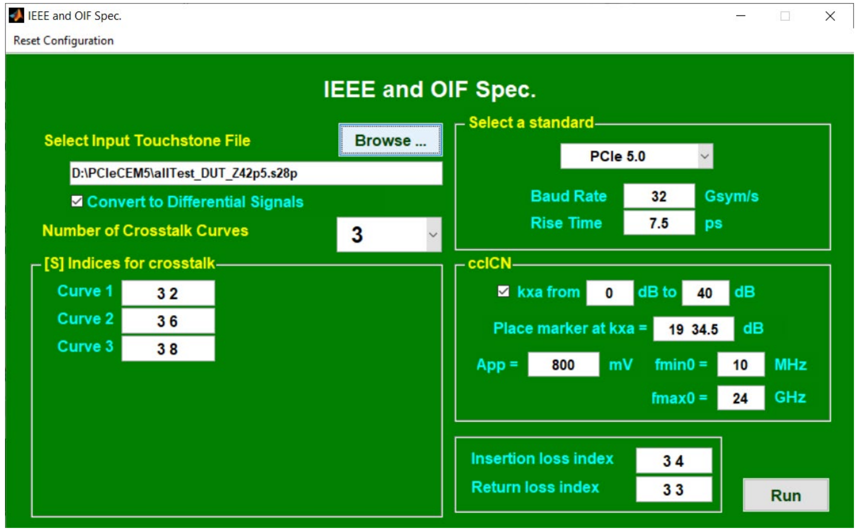
$$ICN = \sqrt{\frac{1}{2} \times df \times \sum_{f_{min}}^{f_{max}} \left\{ \frac{A_{pp}^2}{f_b} \times W(f) \times 10^{\left(\frac{PSXT(f)}{10}\right)} \right\}}$$

$$ccICN = \sqrt{\frac{1}{2} \times df \times \sum_{f_{min}}^{f_{max}} \left\{ \frac{A_{pp}^2}{f_b} \times W(f) \times 10^{\left(\frac{-2\times k_{xa}\times \frac{f}{f_b}}{10}\right)} \times 10^{\left(\frac{PSXT(f)}{10}\right)} \right\}}$$

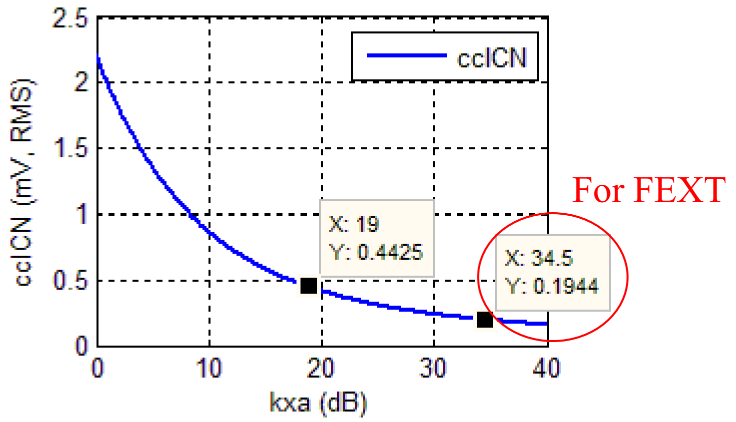
$$W(f) = sinc^2\left(\frac{f}{f_b}\right) \times \frac{1}{1+\left(\frac{f\times t_{rise}}{0.2365}\right)^4} \times \frac{1}{1+\left(\frac{f}{f_r}\right)^8} \quad \text{for} \quad f_{min} < f < f_b$$

$$f_r = 0.75 \times f_b$$

kxa=19dB for $ccICN_{NEXT}$ and kxa=34.5dB for $ccICN_{FEXT}$



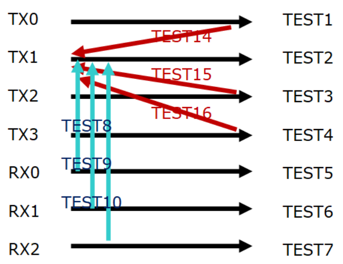
Import ISD results into ADK



Automated batch file (1)

```
# combine
! NEXT
infile D:\PCIeCEM5\Test8.s4p 17 5 19 7
infile D:\PCIeCEM5\Test9.s4p 21 5 23 7
infile D:\PCIeCEM5\Test10.s4p 25 5 27 7
! FEXT
infile D:\PCIeCEM5\Test14.s4p 2 5 4 7
infile D:\PCIeCEM5\Test15.s4p 10 5 12 7
infile D:\PCIeCEM5\Test16.s4p 14 5 16 7
! IL, RL for TX
infile D:\PCIeCEM5\Test1.s4p 1 2 3 4
infile D:\PCIeCEM5\Test2.s4p 5 6 7 8
infile D:\PCIeCEM5\Test3.s4p 9 10 11 12
infile D:\PCIeCEM5\Test4.s4p 13 14 15 16
! IL, RL for RX
infile D:\PCIeCEM5\Test5.s4p 17 18 19 20
infile D:\PCIeCEM5\Test6.s4p 21 22 23 24
infile D:\PCIeCEM5\Test7.s4p 25 26 27 28
outfile D:\PCIeCEM5\allTest.s28p
nports 28
# isd
2x_thru 1
test_coupon D:\PCIeCEM5\thru2x.s4p
dut_fixture D:\PCIeCEM5\allTest.s28p
port_order 2
smooth_dut 3
# reference
infile D:\PCIeCEM5\allTest.s28p_DUT.s28p
outfile D:\PCIeCEM5\allTest_DUT_Z42p5.s28p
zref 42.5
```

Combine multiple .s4p files into one .s28p file



Put IL, RL .s4p files last to have good IL, RL

Run ISD

Set “Smooth DUT ripples” to “Smoothest”

Change reference impedance

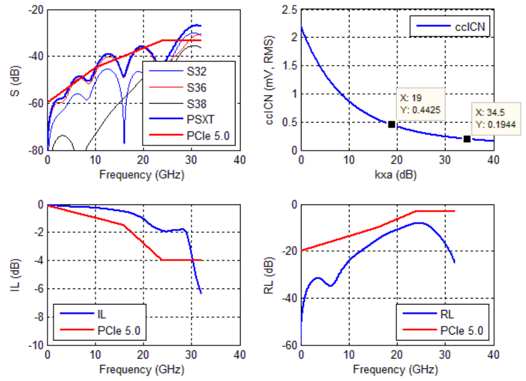
Automated ISD batch file (2)

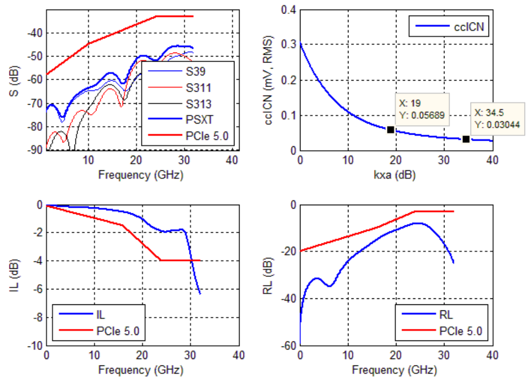
```
# adk "C:\Program Files (x86)\AtaiTec\ADK\adk2.exe"

# standard
infile D:\PCIeCEM5\allTest_DUT_Z42p5.s28p
spec_no 7
differential 1
ccicn 1
il 3 4
rl 3 3
xtalk 3 2
xtalk 3 6
xtalk 3 8
figure_tag ccICN_FEXT
csv_tag ccICN_FEXT

# standard
infile D:\PCIeCEM5\allTest_DUT_Z42p5.s28p
spec_no 7
differential 1
ccicn 1
il 3 4
rl 3 3
xtalk 3 9
xtalk 3 11
xtalk 3 13
figure_tag ccICN_NEXT
csv_tag ccICN_NEXT
```

Make all ADK functions available (License req'd)

Run PCIe 5.0 standard to get ccICN, etc.

Save figures
Save .csv files



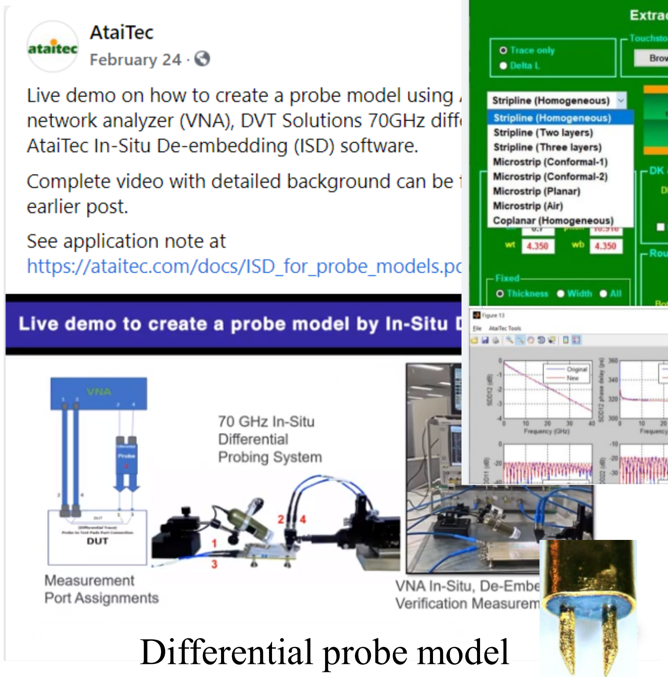


Summary

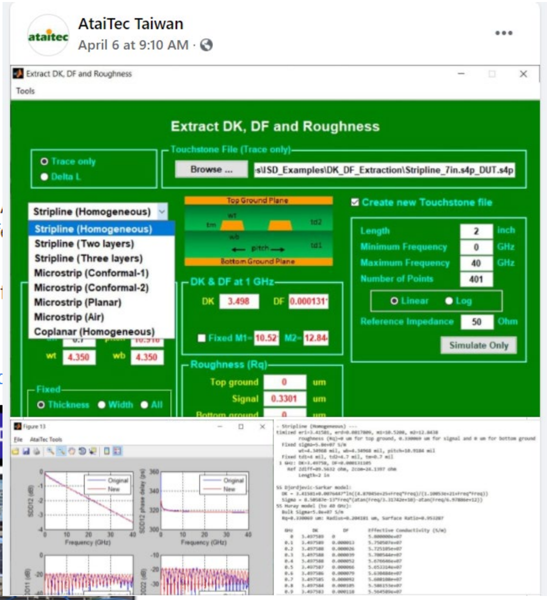
- Accurate de-embedding is crucial for design verification, compliance testing and PCB material property (DK, DF, roughness) extraction.
- Traditional de-embedding methods can give non-causal errors in device-under-test (DUT) results if the test fixture and calibration structure have different impedance.
- In-Situ De-embedding (ISD), with numerous advanced features beyond simply "splitting 2x thru", addresses such impedance difference through software instead of hardware, thereby improving de-embedding accuracy while reducing hardware cost.

To explore more…
Visit Rohde & Schwarz at Booth #1049

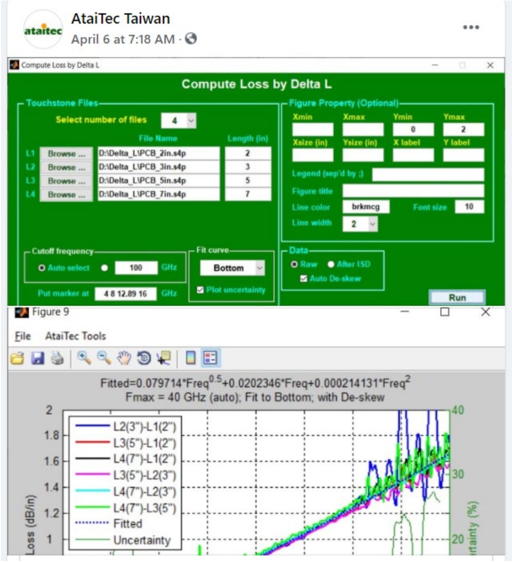
- Follow https://ataitec.com/ and https://www.facebook.com/ataitec



Differential probe model
DVT Solutions, Booth #515



DK/DF/SR extraction



Delta L 4.0